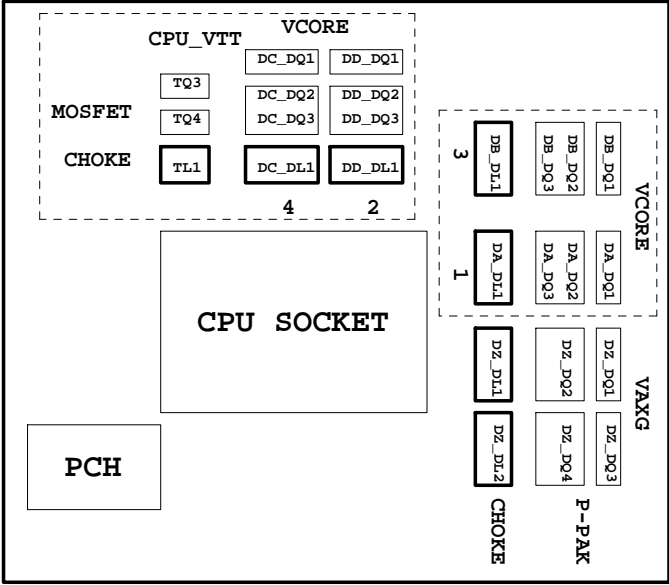


SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*3 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	VT2021 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564
24	VCORE PWM DRIVER IR3598
25	NCP3933 OVER VOLTAGE
26	DISCRETE POWER
27	DDR_15V & CPU_VTT PWM IR3570

SHEET TITLE

28	DDR_15V & CPU_VTT PWM DRIVER CHL8550
29	VCCSA POWER
30	F_PANEL , F_USB2.0/3.0
31	ATX POWER, CLOCK GEN
32	HWM , KB/MS , FAN CTRL
33	LAN ATHEROS AR8151
34	N/A
35	M-SATA
36	DVI
37	HDMI , R_USB30
38	TABLE LIST
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Gigabyte Technology

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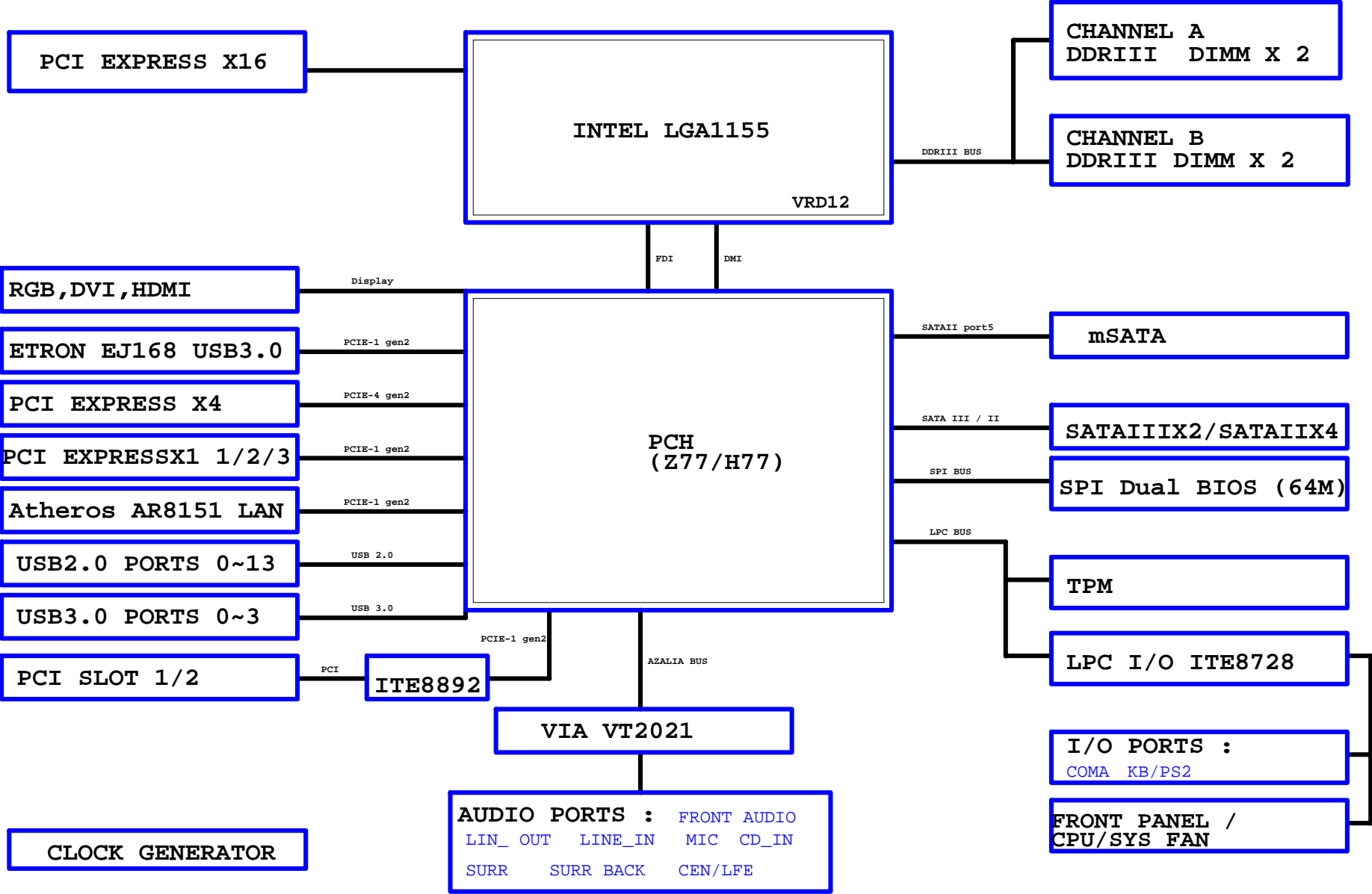
Component value change history

Data	Change Item	Reason
0.1-1124	E-BOM	
02-1216	1. ADD PCH_HS & MOS_HS料號	
	2. PCIE gen2 switch PI3PCIE2415ZHE --> ASM1440	
	3. load-line DAR5=12K , DAR40=1.78K	
10A-0105	1. Z77料號更新	
	2. PWM Driver power vcc or +12v?	
	3. DART2 --> 47K/1/4/S , DAR44 --> 0 ohm	
10B-0113	1. Vcore & VAXG VSEN modify , DAR1,DAR51=100/4/1,DAR2,DAR54=0/4,DAC1,DAC24=3.3mF	
	2. 1.54K加替料:10RC4-001541-22R TA-I	
	1. Remove IR PWM 1X3 pin	
10C-0117	1. DA_DR11,DC_DR11,DZ_DR18 1ohm --> 0ohm	
10D-0119	1. Prochot R65 : 1.65K/4/1 --> 2.74K/4/1	
10E-EVT-0201	1. Modify choke=0.36uH , DRIVER=5V	
10F	1. IR3564要改用新料號03R	
	2. poochot change 100K	
10E-ECN	1. ADD PCB:依利安達	
10T	1. 0 OHM Short-pad	
	2. DDR3 FOR OC 2400MHz UP	
10G	0. PCB Rev1.0 --> ReV1.01	
	1. RS_PWM相關線路移除 (若有上prochot pull up改100 ohm)	
	2. Add M/B ID for DDR3 OC	
	3. 固態電容區分100uF/6.3V & 100uF/16V	
H77-D3H-MVP		
10A-0330	1. PCB H77-D3H REV1.01 --> H77-D3H-MVP REV1.01	
	2. Add Lucid vertune function	

Circuit or PCB layout change

DATE	Change Item	Reason
P67X-UD3-B3		
2011/02/18-0.1	1. 移除LAR11 ,LAR14 , NR28 ,新增NTP11	
2011/02/18-1.0	2. 新增DR388,DR389,DR391 ; Remove DQ49,DR347,DR371 3. CR44改成R0603-RH 4. R1,LAR3,RBR20,LABC25 -->R0402-2-SHORT 5. RAQ1 --> Q_TO223-MASK 6. RARN1 --> R8P4R-0402-SHORT 7. CESD1-5 --> SSOP5 8. RAQ2,RAEC1一起往下移40mil 9. CESD2文字面要標pin1	
2011/03/8-1.01	1. Add "Dolby" logo	
2011/03/8-1.02	1. UAFB1,UAFB2,UBF1,UBF2 Footprint update 1206-->1812 2. Add "AD1" FOR 5VSB	
Z68XP-D3		
1.0	1. update MINI_PCIE footprint 2. 文字面 : SLOT部分全對齊	
Z77-D3H-0.1	EVT	
0.2-1216	1. Remove SE9172 , Add VCC3 內層(注意其他內層power,跨切割) 2. SPDIF AGND --> GND 3. PCI SLOT & PCIEX1/X4 CAP COST DOWN 4. 0 ohm --> SHORT PAD 5. REMOVE SMBUS FROM COMP TO SOLDER SIDE IN DR POWER 6. SATA3 connect Change to 90 degree (記得SATA3訊號部分要做挖空) 7. Add "108dB"文字面 8. Remove VCC1_05_PCH & VCC1_8_PCH gate net 9. Add EJ168 R_USB30_1 & F_USB3 10. UAE1/UAE2 NET SWAP 11. 內層+12V要打VIA在COMA處 12. SPDIFO_HDMI走12mil	
1.0	1. SATA2~SATA3文字面要隱藏 2. DART2 移至 DC_DQ1左上方 3. Q7 & DAR31 NET Change	
1.01	1. 0 OHM SHORT PAD (LAN & AUDIO) 2. DDR3 2400MHz OC modify	

BLOCK DIAGRAM





LGA1155A

M_AAA0	AV27	SA_MA[0]
M_AAA1	AY24	SA_MA[1]
M_AAA2	AW24	SA_MA[2]
M_AAA3	AW23	SA_MA[3]
M_AAA4	AV23	SA_MA[4]
M_AAA5	AT24	SA_MA[5]
M_AAA6	AT23	SA_MA[6]
M_AAA7	AU22	SA_MA[7]
M_AAA8	AV22	SA_MA[8]
M_AAA9	AT22	SA_MA[9]
M_AAA10	AV28	SA_MA[10]
M_AAA11	AU21	SA_MA[11]
M_AAA12	AT21	SA_MA[12]
M_AAA13	AW32	SA_MA[13]
M_AAA14	AU20	SA_MA[14]
M_AAA15	AT20	SA_MA[15]

[7] M_SWEA	M_SWEA	AW29	SA_WE#
[7] M_SCASA	M_SCASA	AV30	SA_CAS#
[7] M_SRASA	M_SRASA	AU28	SA_RAS#
[7] M_SBAA0	M_SBAA0	AY29	SA_BS[0]
[7] M_SBAA1	M_SBAA1	AW28	SA_BS[1]
[7] M_SBAA2	M_SBAA2	AV20	SA_BS[2]

[7] M-CSA0	M-CSA0	AU29	SA_CS#
[7] M-CSA1	M-CSA1	AV32	SA_CS#
[7] M-CSA2	M-CSA2	AW30	SA_CS#
[7] M-CSA3	M-CSA3	AU33	SA_CS#

[7] M-CKEA0	M-CKEA0	AV19	SA_CKE[0]
[7] M-CKEA1	M-CKEA1	AT19	SA_CKE[1]
[7] M-CKEA2	M-CKEA2	AU18	SA_CKE[2]
[7] M-CKEA3	M-CKEA3	AV18	SA_CKE[3]

M_ODT_A0	AV31	SA_ODT[0]
M_ODT_A1	AU32	SA_ODT[1]
M_ODT_A2	AU30	SA_ODT[2]
M_ODT_A3	AW33	SA_ODT[3]

[7] M-DCLKA0	M-DCLKA0	AY25	SA_CK[0]
[7] M-DCLKA0	M-DCLKA0	AW25	SA_CK[0]
[7] M-DCLKA1	M-DCLKA1	AU24	SA_CK[1]
[7] M-DCLKA1	M-DCLKA1	AU25	SA_CK[1]
[7] M-DCLKA2	M-DCLKA2	AW27	SA_CK[2]
[7] M-DCLKA2	M-DCLKA2	AY27	SA_CK[2]
[7] M-DCLKA3	M-DCLKA3	AU26	SA_CK[3]
[7] M-DCLKA3	M-DCLKA3	AW26	SA_CK[3]

[7,8] M_DDR3_RST	M_DR1	AW18	SM_DRAMRST#
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MBC8	0.1u/4/X7R/16V/K/X	
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AV13	SA_DQS[8]
AV12	SA_DQS#
AU12	SA_ECC_CB[0]
AU14	SA_ECC_CB[1]
AW13	SA_ECC_CB[2]
AY13	SA_ECC_CB[3]
AU13	SA_ECC_CB[4]
AY12	SA_ECC_CB[5]
AW12	SA_ECC_CB[6]

DDR_0

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LGA1155[10SC1-F01155-01R]

AK3	M_DQSA0
AK2	M_DQSA0
AJ3	M_DA0
AJ4	M_DA1
AL3	M_DA2
AL4	M_DA3
AJ2	M_DA4
AJ1	M_DA5
AL2	M_DA6
AL1	M_DA7

AP3	M_DQSA1
AP2	M_DQSA1

AN1	M_DA8
AN4	M_DA9
AR3	M_DA10
AR4	M_DA11
AN2	M_DA12
AN3	M_DA13
AR2	M_DA14
AR1	M_DA15

AW4	M_DQSA2
AW4	M_DQSA2

AV2	M_DA16
AW3	M_DA17
AV5	M_DA18
AW5	M_DA19
AU2	M_DA20
AJ3	M_DA21
AJ5	M_DA22
AY5	M_DA23

AV8	M_DQSA3
AW8	M_DQSA3

AY7	M_DA24
AU7	M_DA25
AV9	M_DA26
AU9	M_DA27
AV7	M_DA28
AW7	M_DA29
AW9	M_DA30
AY9	M_DA31

AV37	M_DQSA4
AV36	M_DQSA4

AU35	M_DA32
AW37	M_DA33
AU39	M_DA34
AU36	M_DA35
AY35	M_DA36
AY36	M_DA37
AU38	M_DA38
AU37	M_DA39

AP38	M_DQSA5
AP39	M_DQSA5

AR40	M_DA40
AR37	M_DA41
AN38	M_DA42
AN37	M_DA43
AR39	M_DA44
AR38	M_DA45
AN39	M_DA46
AN40	M_DA47

AK38	M_DQSA6
AK39	M_DQSA6

AL40	M_DA48
AL37	M_DA49
AJ38	M_DA50
AJ37	M_DA51
AL39	M_DA52
AL38	M_DA53
AJ39	M_DA54
AJ40	M_DA55

AF38	M_DQSA7
AF39	M_DQSA7

AG40	M_DA56
AG37	M_DA57
AE38	M_DA58
AE37	M_DA59
AG39	M_DA60
AG38	M_DA61
AE39	M_DA62
AE40	M_DA63

[7] M_ODT_A[0..3] < M_ODT_A[0..3]

[8] M_ODT_B[0..3] < M_ODT_B[0..3]

[7] M_DA[0..63] < M_DA[0..63]

[8] M_DB[0..63] < M_DB[0..63]

[7] M_DQSA[0..7] < M_DQSA[0..7]

[7] M_DQSA[0..7] < M_DQSA[0..7]

[7] M_AA[0..15] < M_AA[0..15]

[8] M_AAB[0..15] < M_AAB[0..15]

[8] M_DQSB[0..7] < M_DQSB[0..7]

[8] M_DQSB[0..7] < M_DQSB[0..7]

LGA1155B

M_AAB0	AK24	SB_MA[0]
M_AAB1	AM20	SB_MA[1]
M_AAB2	AM19	SB_MA[2]
M_AAB3	AK18	SB_MA[3]
M_AAB4	AP19	SB_MA[4]
M_AAB5	AP18	SB_MA[5]
M_AAB6	AM18	SB_MA[6]
M_AAB7	AL18	SB_MA[7]
M_AAB8	AY17	SB_MA[8]
M_AAB9	AY17	SB_MA[9]
M_AAB10	AN23	SB_MA[10]
M_AAB11	AU17	SB_MA[11]
M_AAB12	AT18	SB_MA[12]
M_AAB13	AR26	SB_MA[13]
M_AAB14	AY16	SB_MA[14]
M_AAB15	AV16	SB_MA[15]

[8] M_SWEB	M_SWEB	AR25	SB_WE#
[8] M_SCASB	M_SCASB	AK25	SB_CAS#
[8] M_SRASB	M_SRASB	AP24	SB_RAS#

[8] M_SBAB0	M_SBAB0	AP23	SB_BS[0]
[8] M_SBAB1	M_SBAB1	AM26	SB_BS[1]
[8] M_SBAB2	M_SBAB2	AW17	SB_BS[2]

[8] M-CSB0	M-CSB0	AN25	SB_CS#
[8] M-CSB1	M-CSB1	AN26	SB_CS#
[8] M-CSB2	M-CSB2	AL26	SB_CS#
[8] M-CSB3	M-CSB3	AT26	SB_CS#

[8] M-CKEB0	M-CKEB0	AU16	SB_CKE[0]
[8] M-CKEB1	M-CKEB1	AY15	SB_CKE[1]
[8] M-CKEB2	M-CKEB2	AW15	SB_CKE[2]
[8] M-CKEB3	M-CKEB3	AV15	SB_CKE[3]

M_ODT_B0	AL26	SB_ODT[0]
M_ODT_B1	AP26	SB_ODT[1]
M_ODT_B2	AM26	SB_ODT[2]
M_ODT_B3	AK26	SB_ODT[3]

[8] M-DCLKB0	M-DCLKB0	AL21	SB_CK[0]
[8] M-DCLKB0	M-DCLKB0	AL22	SB_CK[0]
[8] M-DCLKB1	M-DCLKB1	AK20	SB_CK[1]
[8] M-DCLKB2	M-DCLKB2	AL23	SB_CK[2]
[8] M-DCLKB2	M-DCLKB2	AM22	SB_CK[2]
[8] M-DCLKB3	M-DCLKB3	AP21	SB_CK[3]
[8] M-DCLKB3	M-DCLKB3	AN21	SB_CK[3]

[8] M_VREF_DQB	M_VREF_DQB	AH1	FC_AH1
[7] M_VREF_DQA	M_VREF_DQA	AH4	FC_AH4

AN16	SB_DQS[8]
AN15	SB_DQS#
AN16	SB_ECC_CB[0]
AN16	SB_ECC_CB[1]
AN16	SB_ECC_CB[2]
AN15	SB_ECC_CB[3]
AN15	SB_ECC_CB[4]
AN15	SB_ECC_CB[5]
AN15	SB_ECC_CB[6]

AP32	M_DB40
AP21	M_DB41
AP35	M_DB42
AP34	M_DB43
AP32	M_DB44
AR31	M_DB45
AR35	M_DB46
AR34	M_DB47

AL33	M_DQSB6
AM33	M_DQSB6

AM32	M_DB48
AM31	M_DB49
AL35	M_DB50
AL32	M_DB51
AM34	M_DB52
AL31	M_DB53
AM35	M_DB54
AL34	M_DB55

AG35	M_DQSB7
AG34	M_DQSB7

AH35	M_DB56
AH34	M_DB57
AE34	M_DB58
AE35	M_DB59
AJ35	M_DB60
AJ34	M_DB61
AF33	M_DB62
AF35	M_DB63

DDR_1

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LGA1155[10SC1-F01155-01R]

AH7	M_DQSB0
AH6	M_DQSB0
AG7	M_DB0
AG8	M_DB1
AJ9	M_DB2
AJ8	M_DB3
AG5	M_DB4
AG6	M_DB5
AJ6	M_DB6
AJ7	M_DB7

AM8	M_DQSB1
AL8	M_DQSB1

AL7	M_DB8
AM7	M_DB9
AM10	M_DB10
AL10	M_DB11
AL6	M_DB12
AM6	M_DB13
AL9	M_DB14
AM9	M_DB15

AR8	M_DQSB2
AP8	M_DQSB2

AF7	M_DB16
AR7	M_DB17
AP10	M_DB18
SB_DQ[19]	M_DB19
AP6	M_DB20
AR6	M_DB21
AP9	M_DB22
AR9	M_DB23

AN13	M_DQSB3
AN12	M_DQSB3

AM12	M_DB24
AM13	M_DB25
AR13	M_DB26
AP13	M_DB27
AL12	M_DB28
AL13	M_DB29
AR12	M_DB30
AP12	M_DB31

AN29	M_DQSB4
AN28	M_DQSB4

AR28	M_DB32
AR29	M_DB33
AL28	M_DB34
AL29	M_DB35
AP28	M_DB36
AP29	M_DB37
AM28	M_DB38
AM29	M_DB39

AP33	M_DQSB5
AR33	M_DQSB5

AP32	M_DB40
AP21	M_DB41
AP35	M_DB42
AP34	M_DB43
AP32	M_DB44
AR31	M_DB45
AR35	M_DB46
AR34	M_DB47

AL33	M_DQSB6
AM33	M_DQSB6

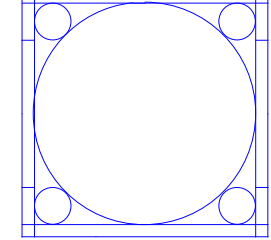
AM32	M_DB48
AM31	M_DB49
AL35	M_DB50
AL32	M_DB51
AM34	M_DB52
AL31	M_DB53
AM35	M_DB54
AL34	M_DB55

AG35	M_DQSB7
AG34	M_DQSB7

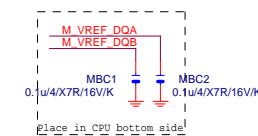
AH35	M_DB56
AH34	M_DB57
AE34	M_DB58
AE35	M_DB59
AJ35	M_DB60
AJ34	M_DB61
AF33	M_DB62
AF35	M_DB63

LGA1155

ILM BP/1156/CSP



Need check the new CPU ME

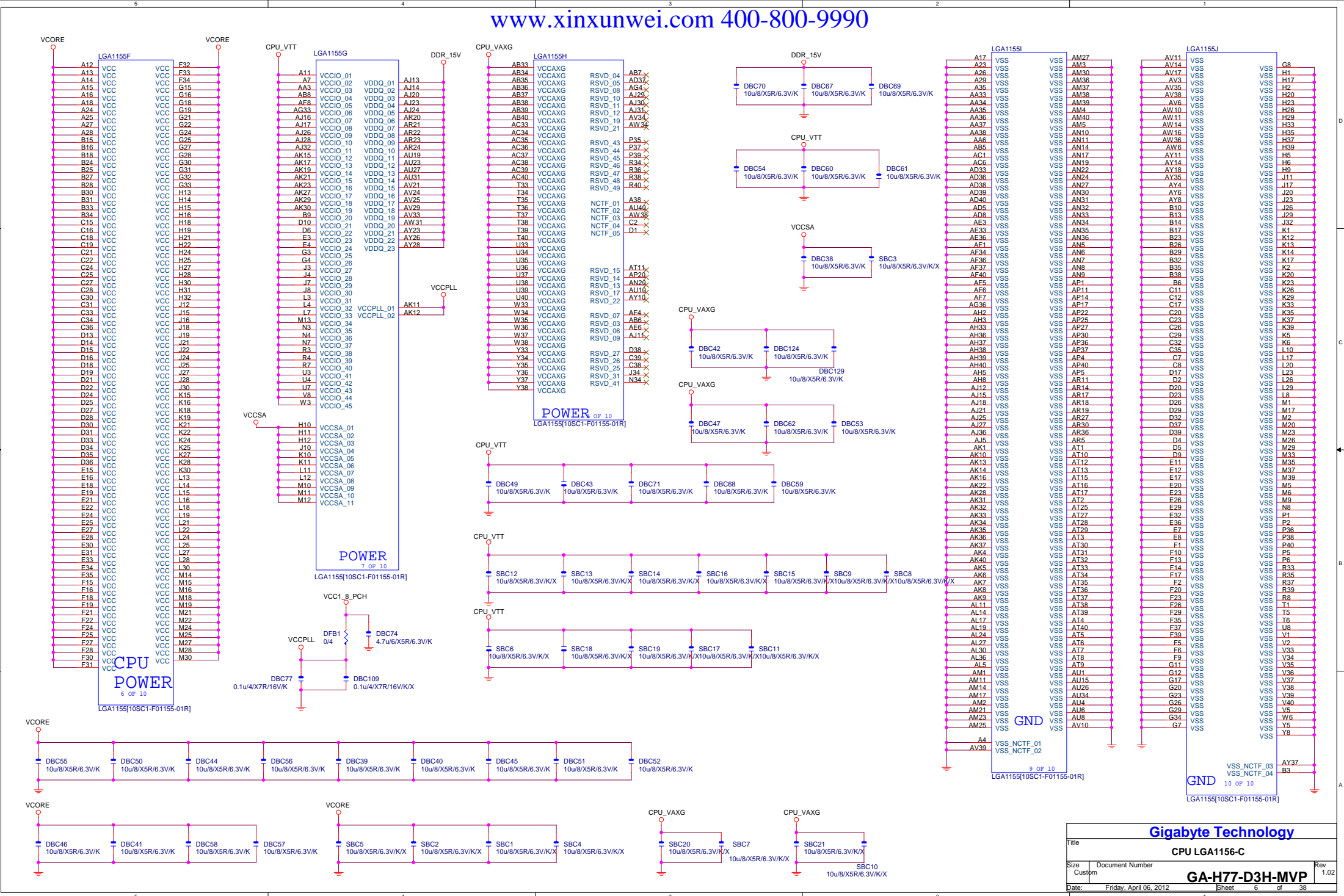


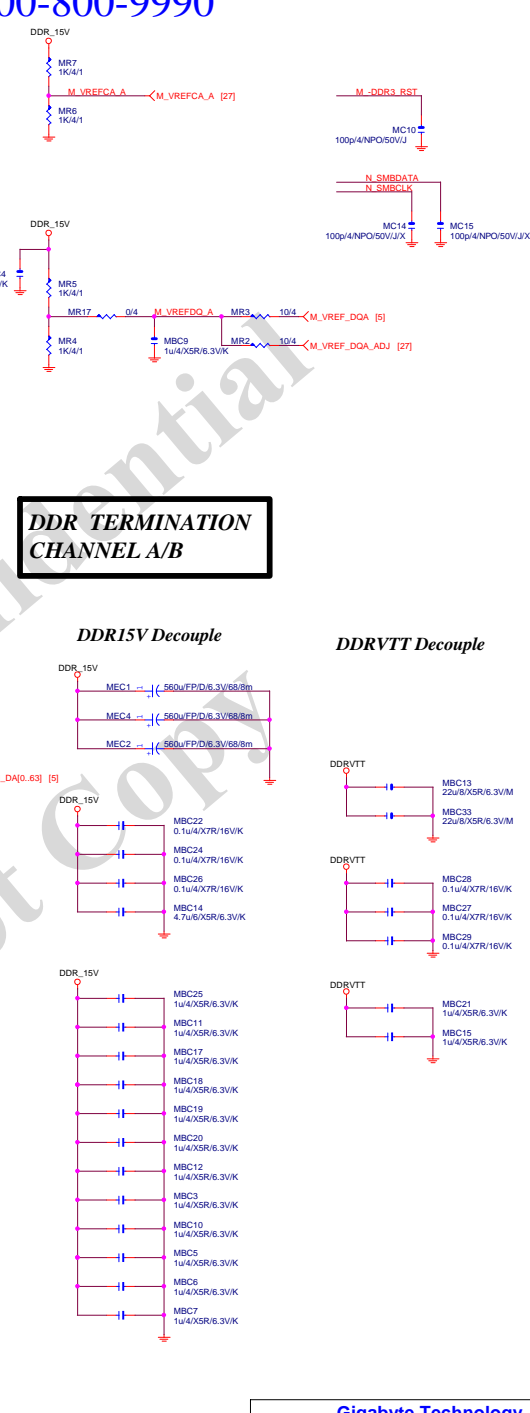
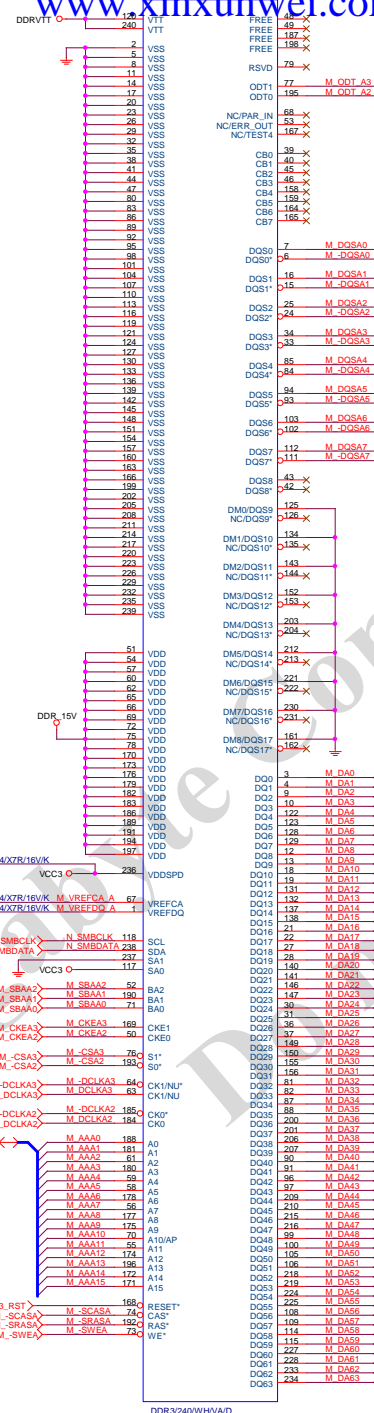
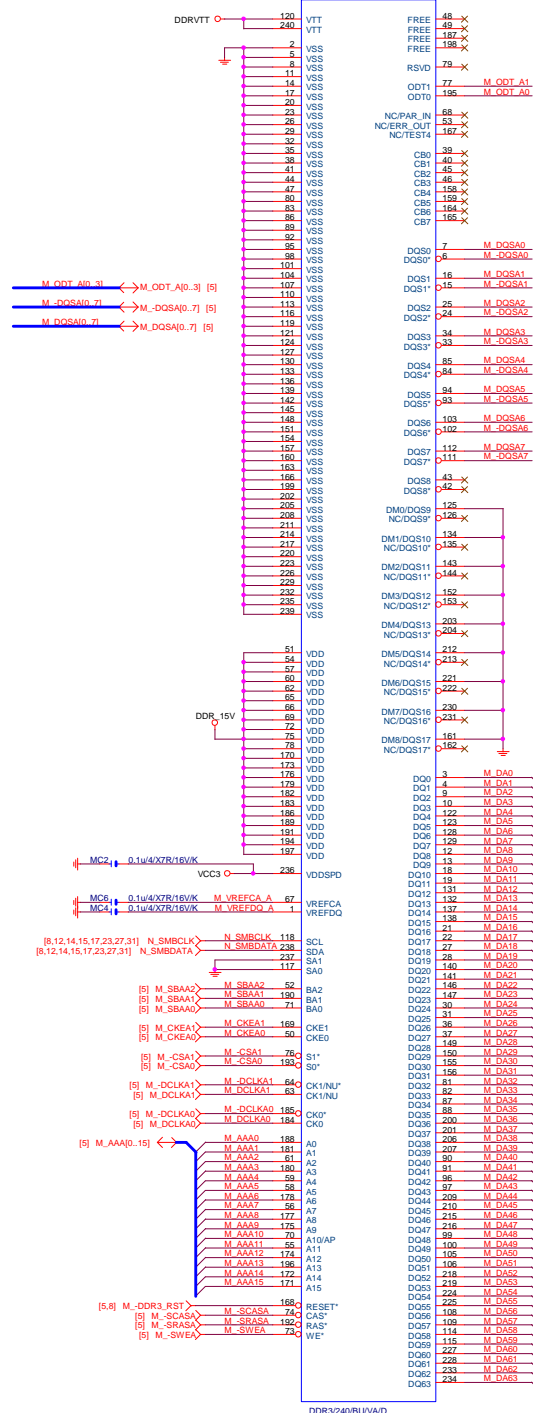
Gigabyte Technology

CPU LGA1156-B

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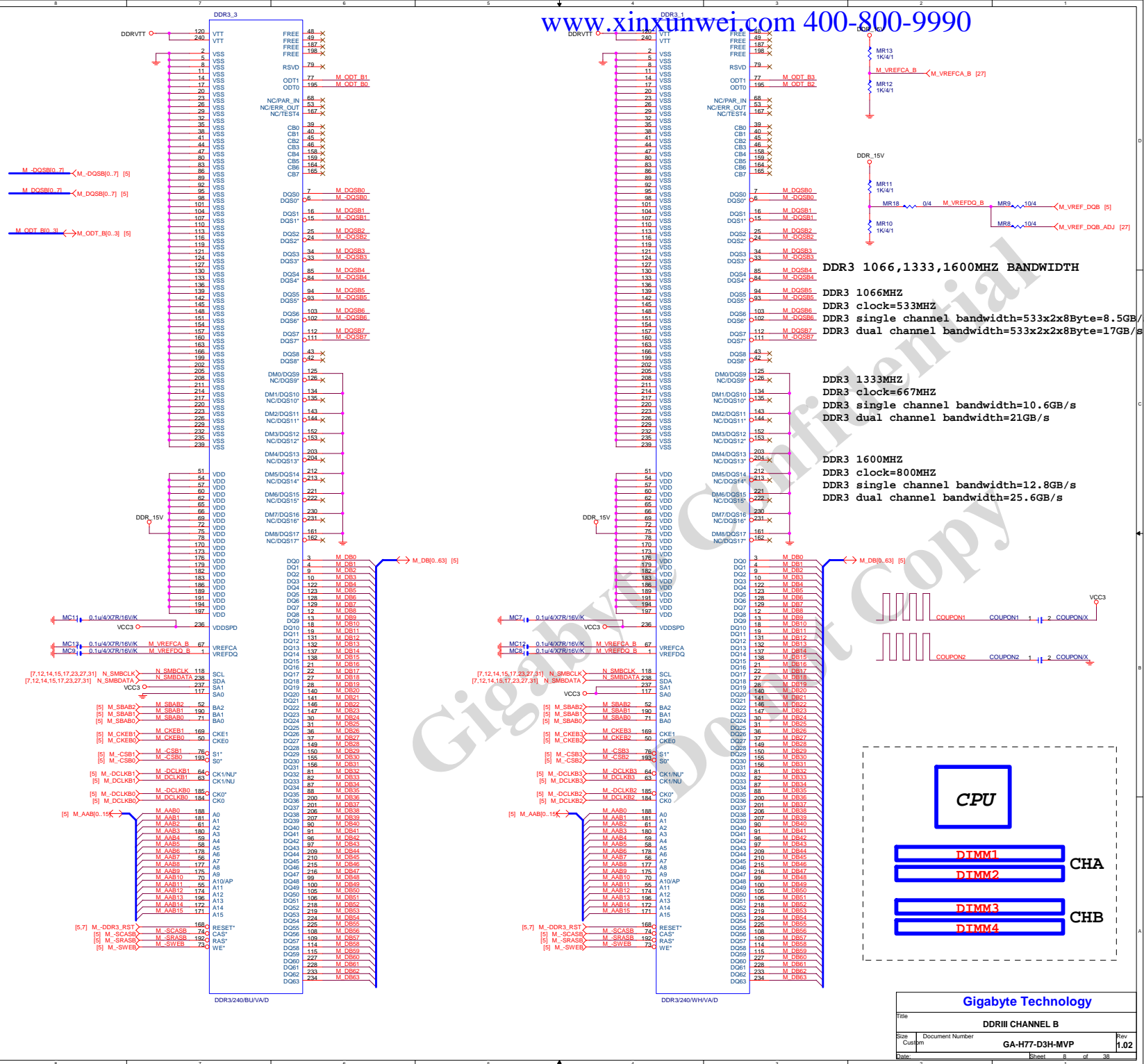


DDR TERMINATION CHANNEL A/B

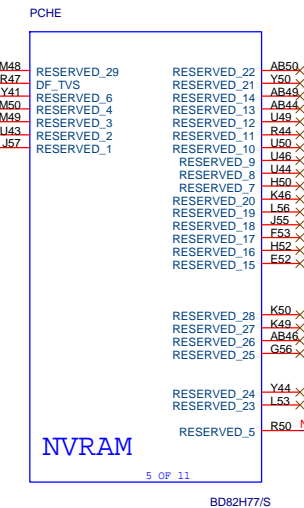
DDR15V Decouple

DDRVTT Decouple

Gigabyte Technology			
Title			
DDRIII CHANNEL A			
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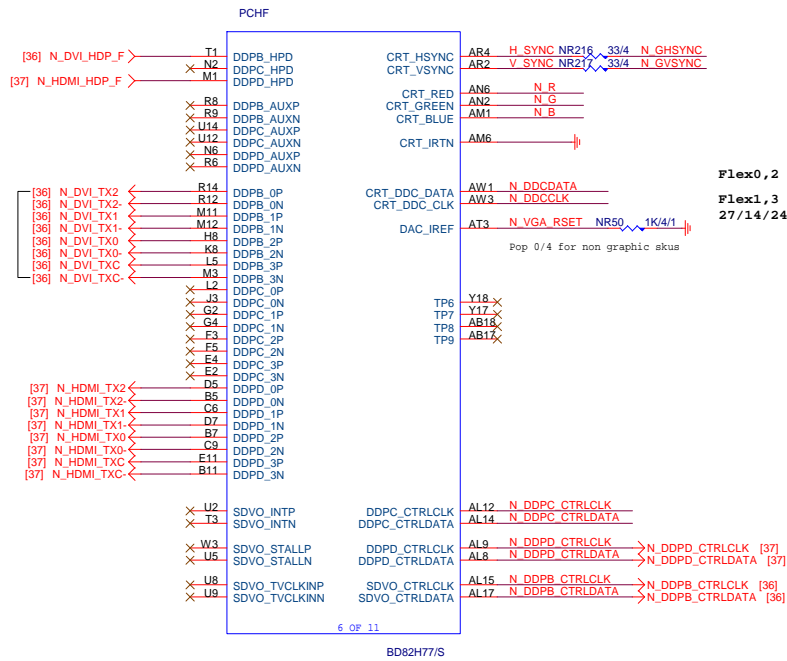
USB 0:20/5/7/5/20 (breakout min
 8/4/4/4/8) ; ONLY 3 VIAS
 Impedance=85 +/- 17.5%
 Back Panel < 10000 MILS
 Front Panel < 6000 MILS



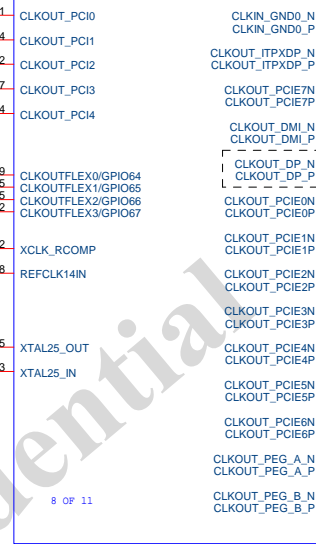
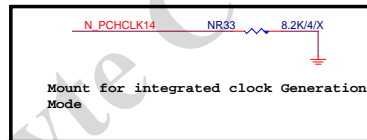
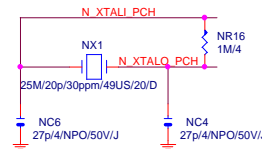
USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

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Title			
PCH FDI,DMI,USB ,PCIE			
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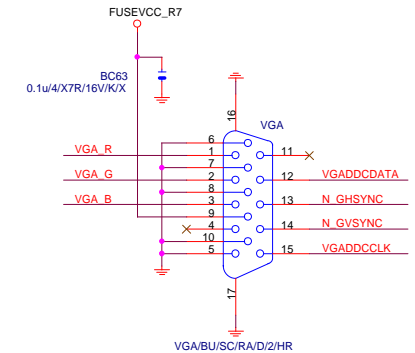
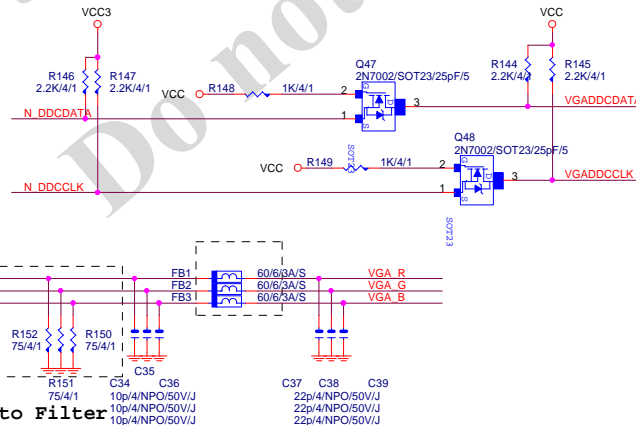
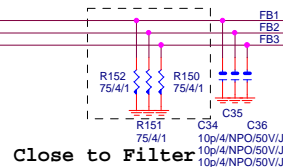
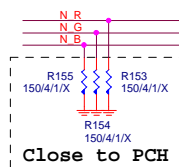
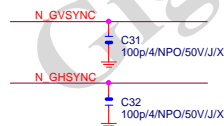
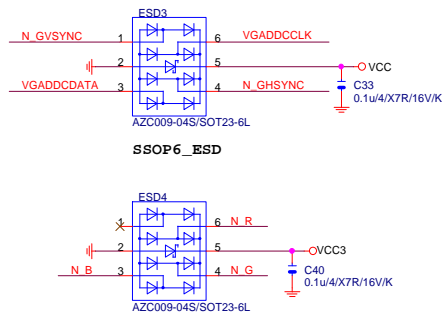


Flex0,2 : 33MHZ
Flex1,3 : 27/14/24/48/25MHZ



Differential Clock:18/4/6/4/18
Impedance=90 +- 15%

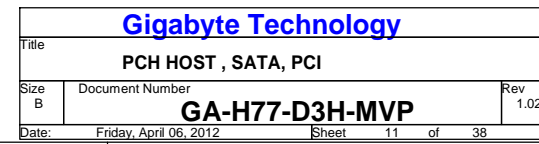
Check if NC for P67 non graphic chip



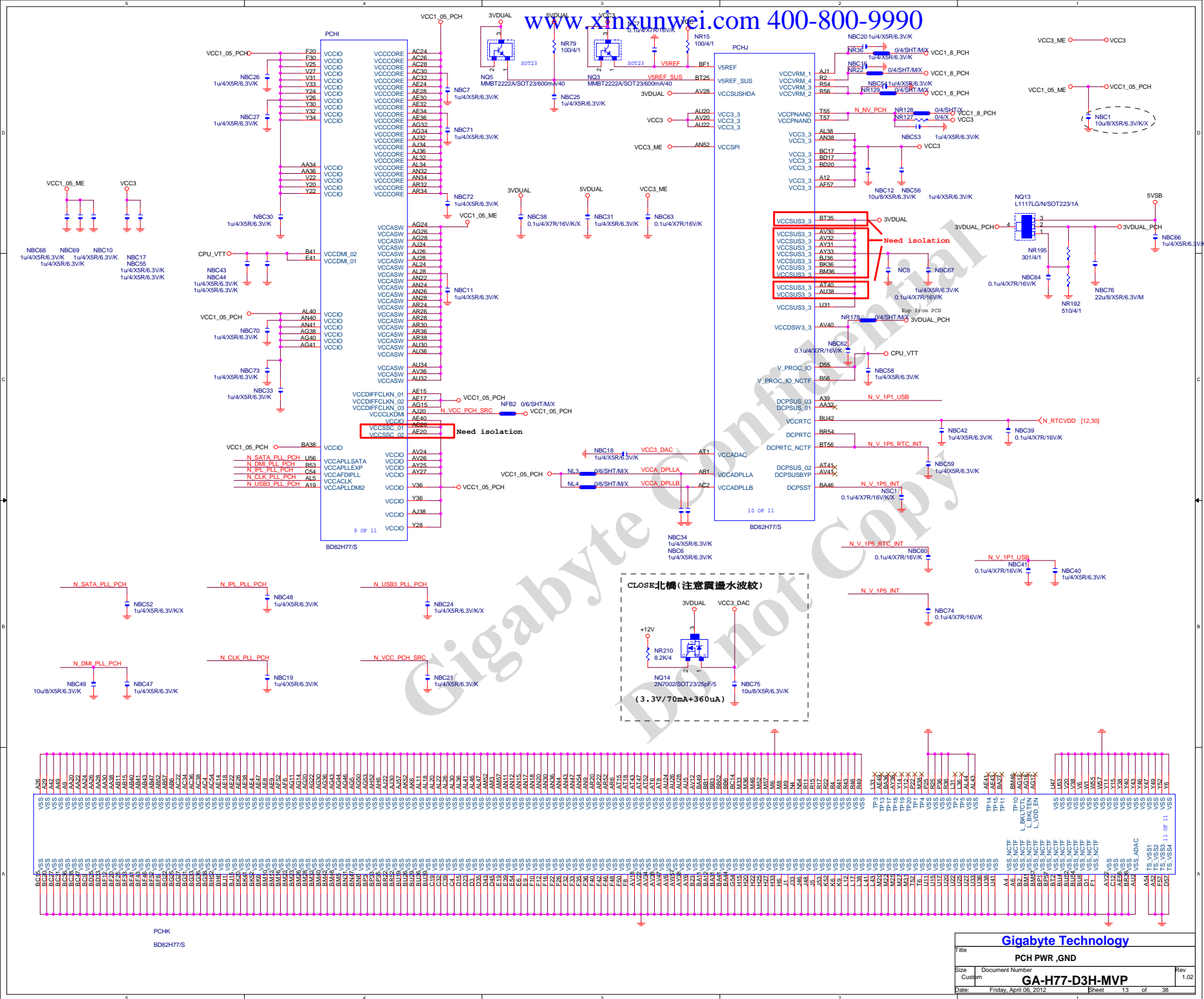
Gigabyte Technology

Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number	Rev	
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NR64 8.2K/4/X N_GPIO17
NR173 8.2K/4/X N_GPIO19



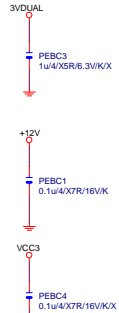
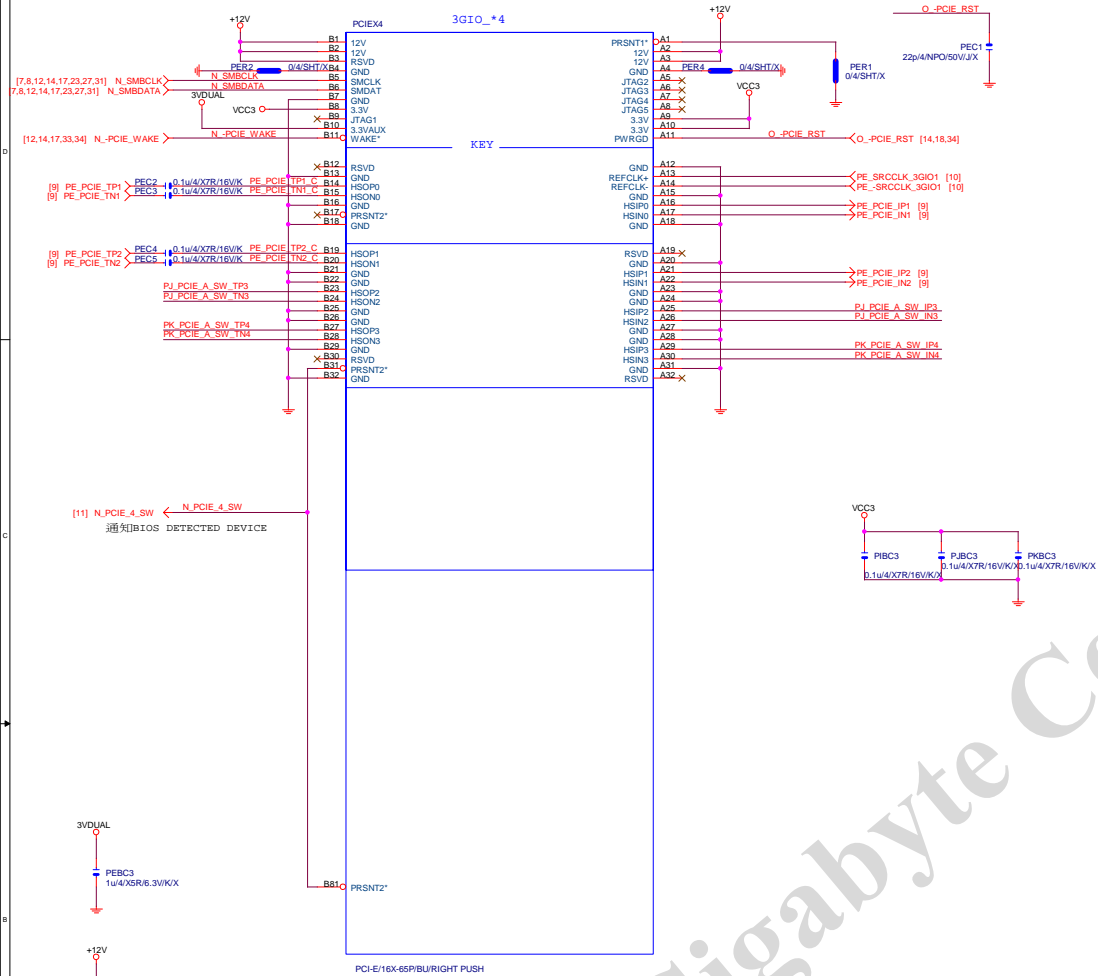






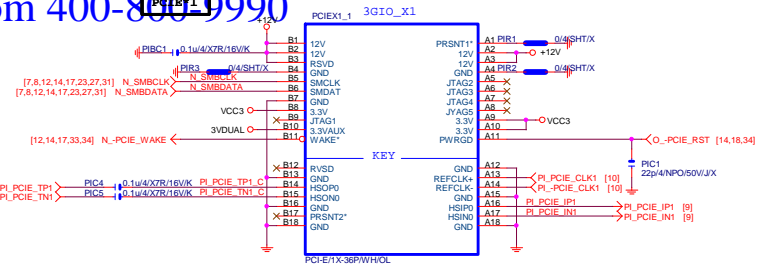
PCI-E REV:2.0--> 5GHZ

PCIE*4

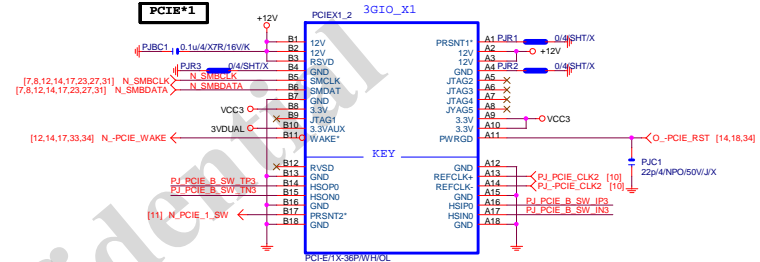


	N_PCIE_4_SW (PCH GPIO38)	PCIE4_X1 (SIO_GPIO26)
PCIE1_1/PCIE1_3	H	H
PCIE1_2/PCIE1_4	H	H
PCIE1_3/PCIE1_5	L	L

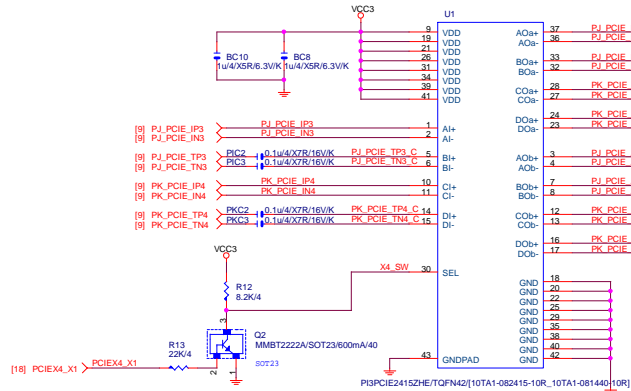
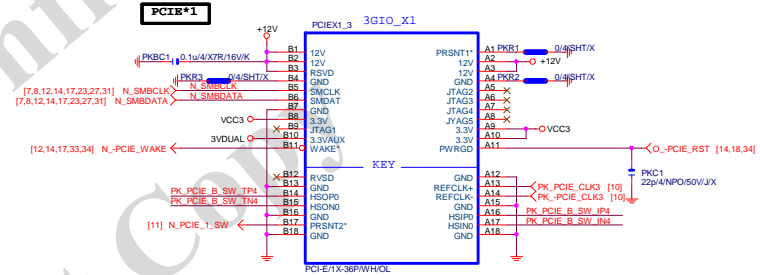
PCIE*1



PCIE*1



PCIE*1



Function	SEL
X1--> x0a	L, PCIE4 SLOT-->X1
X1--> x0b	H, PCIE4 SLOT-->X4

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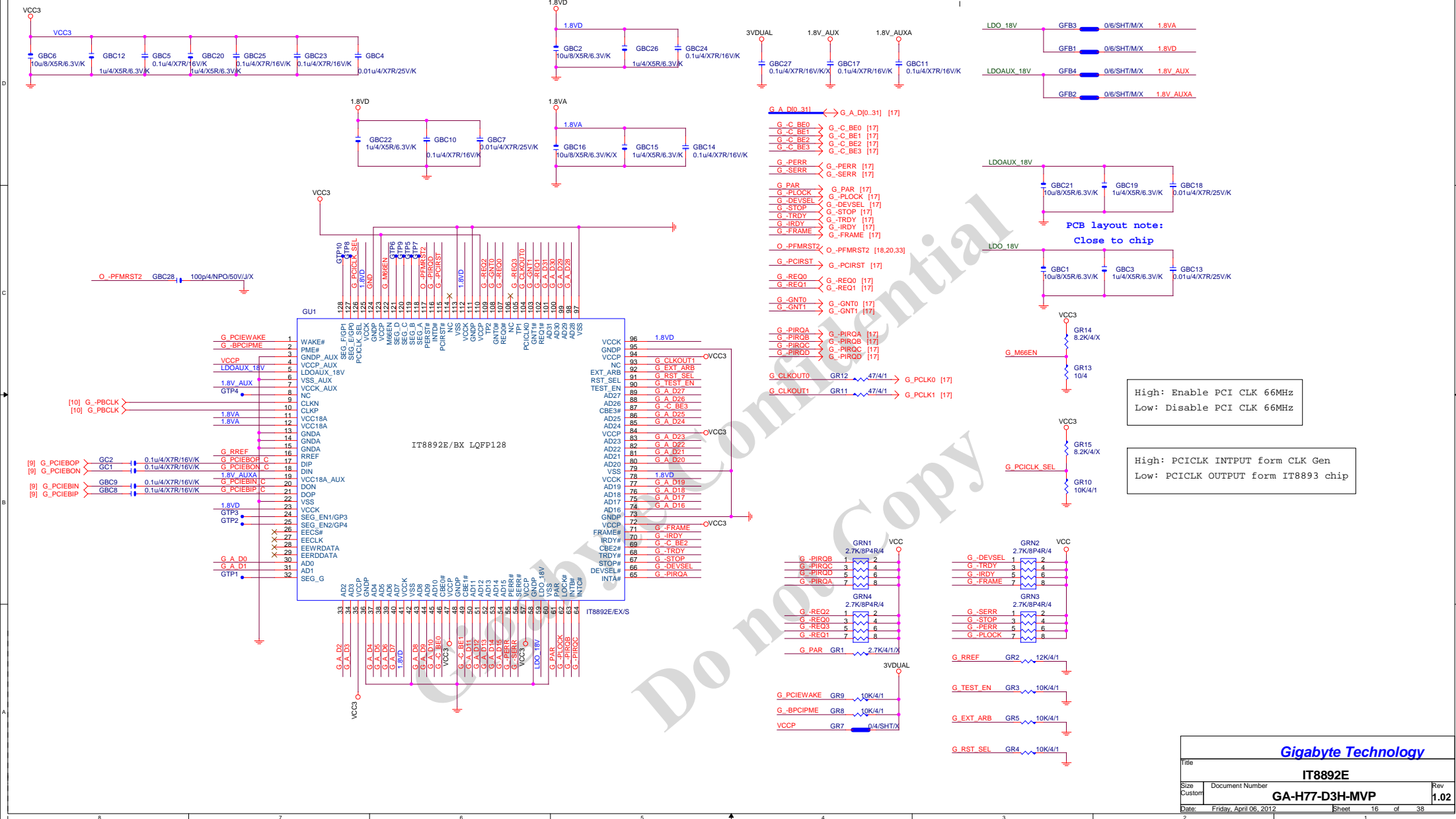
PCIE X1 1.2

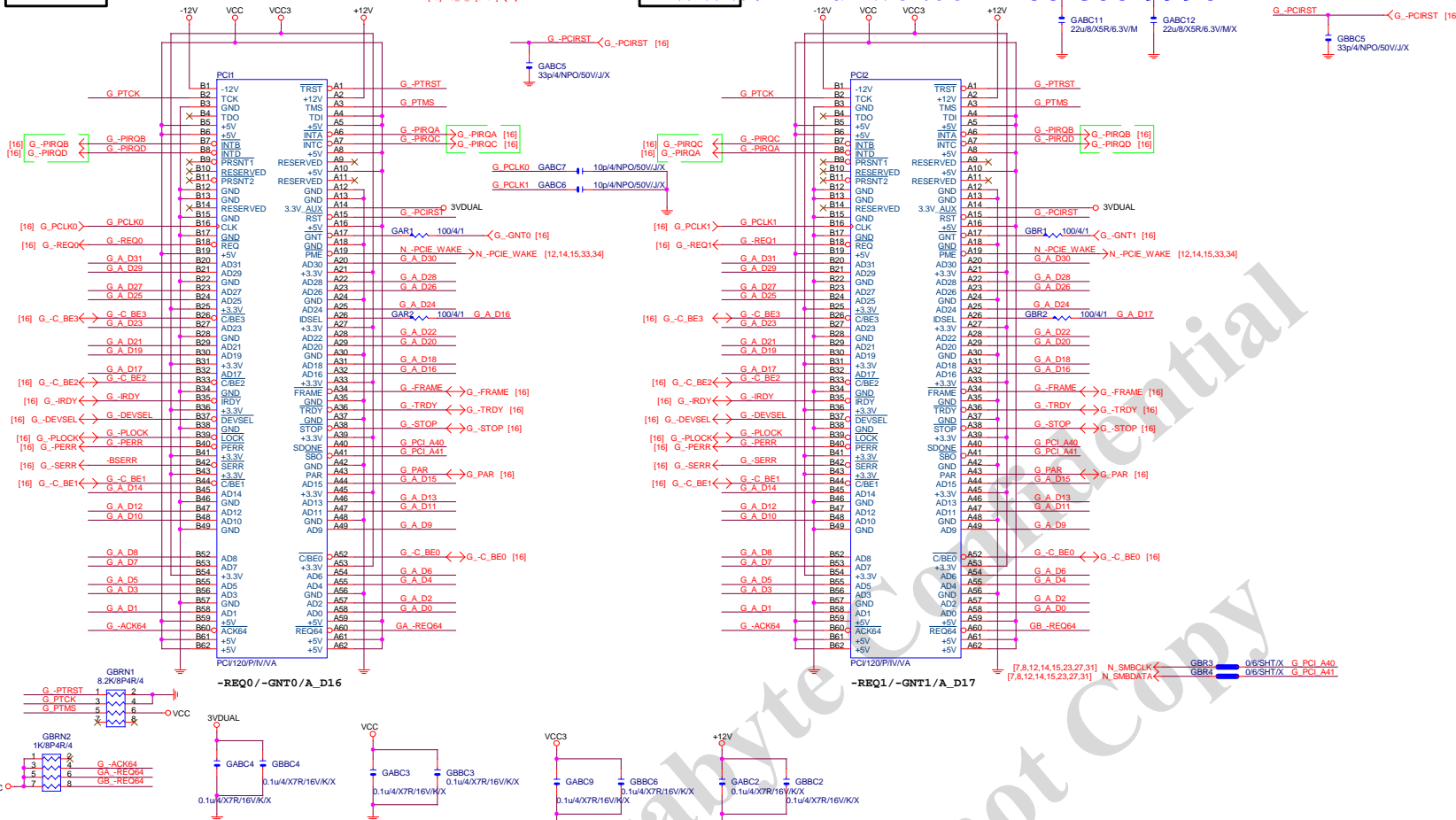
GA-H77-D3H-MVP

Rev 1.02

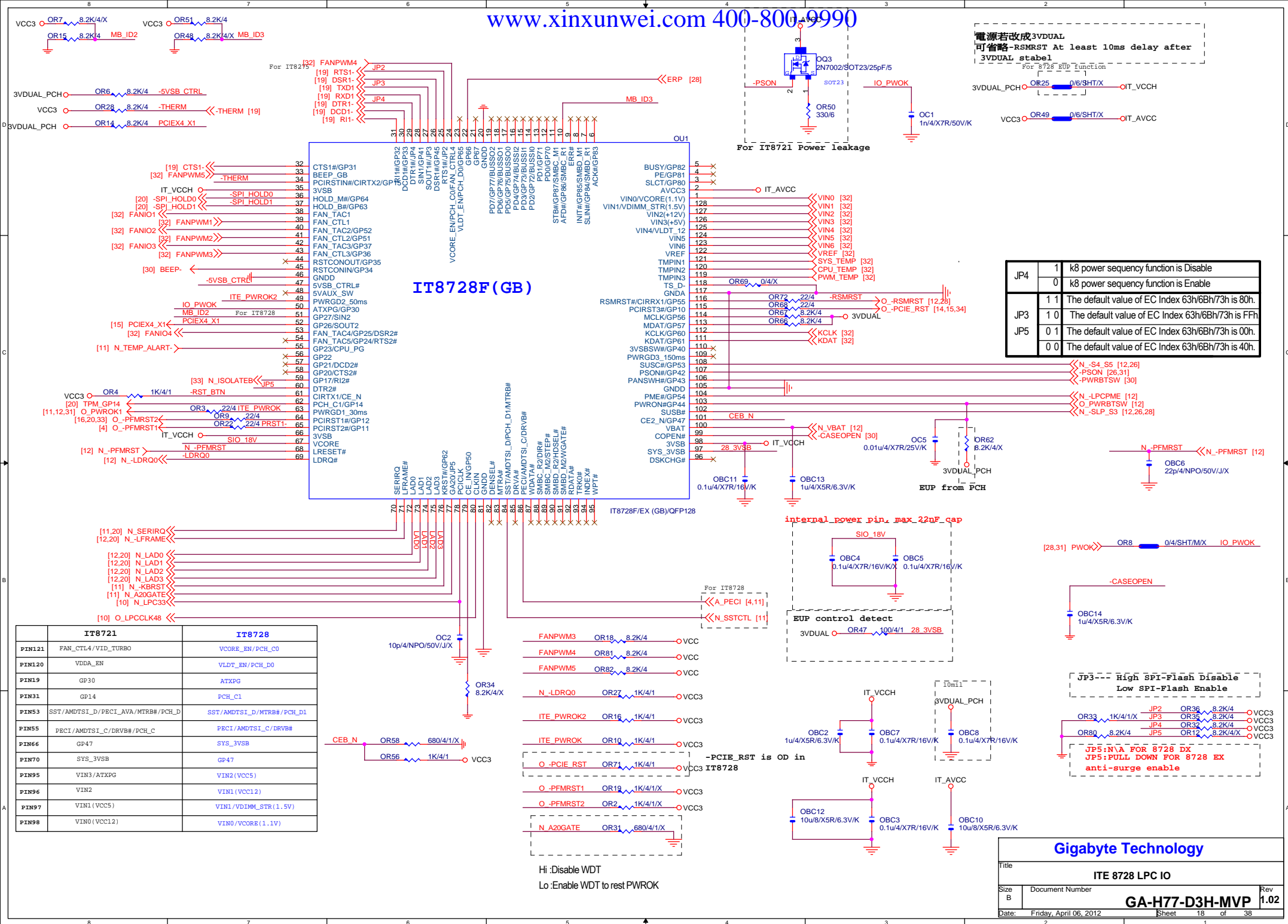
Date: Friday, April 06, 2012

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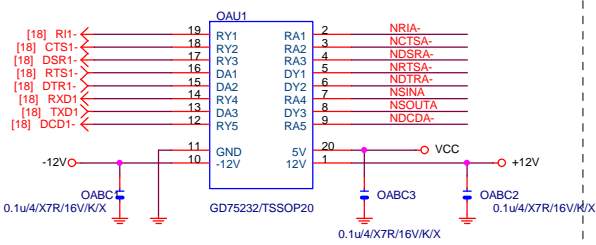




GIGABYTE™			
Title			
PCI SLOT 1&2			
Size	Document Number	Rev	
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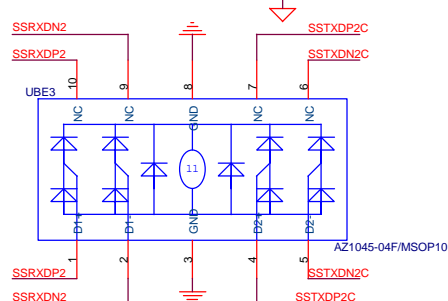
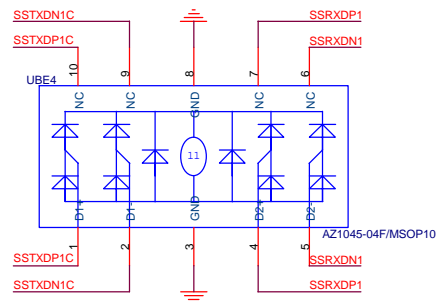
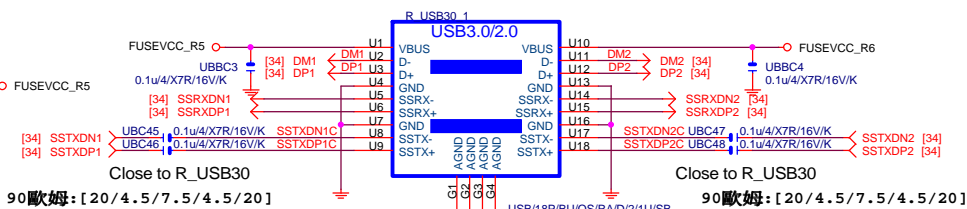
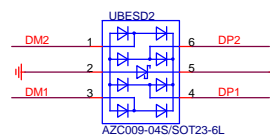
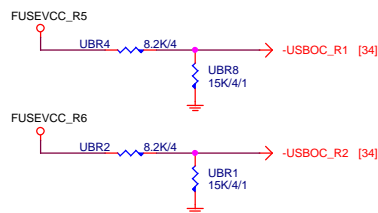
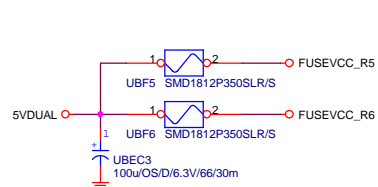
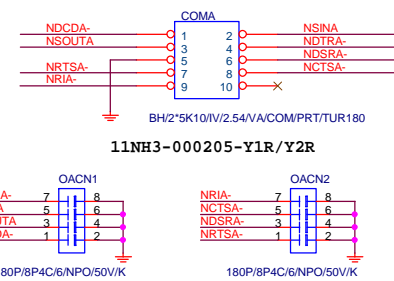
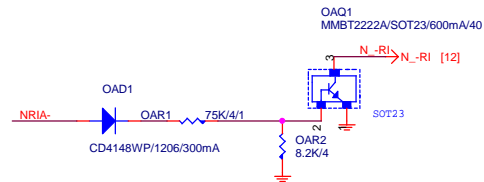


COMA



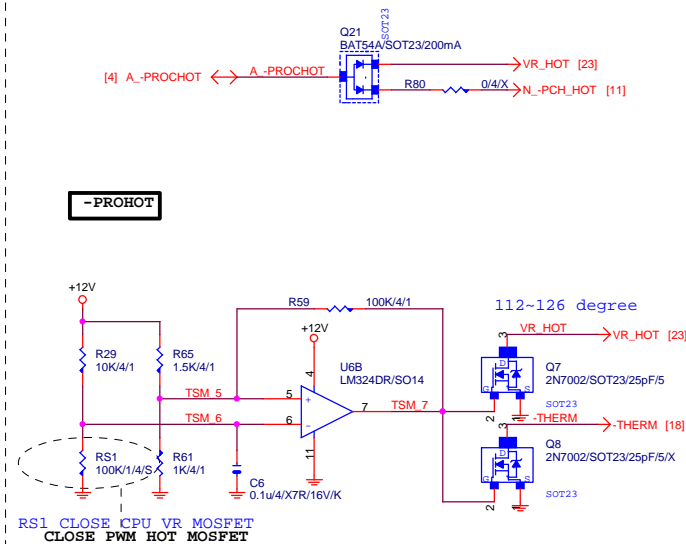
www.xinxunwei.com 400-800-9990

COM R1



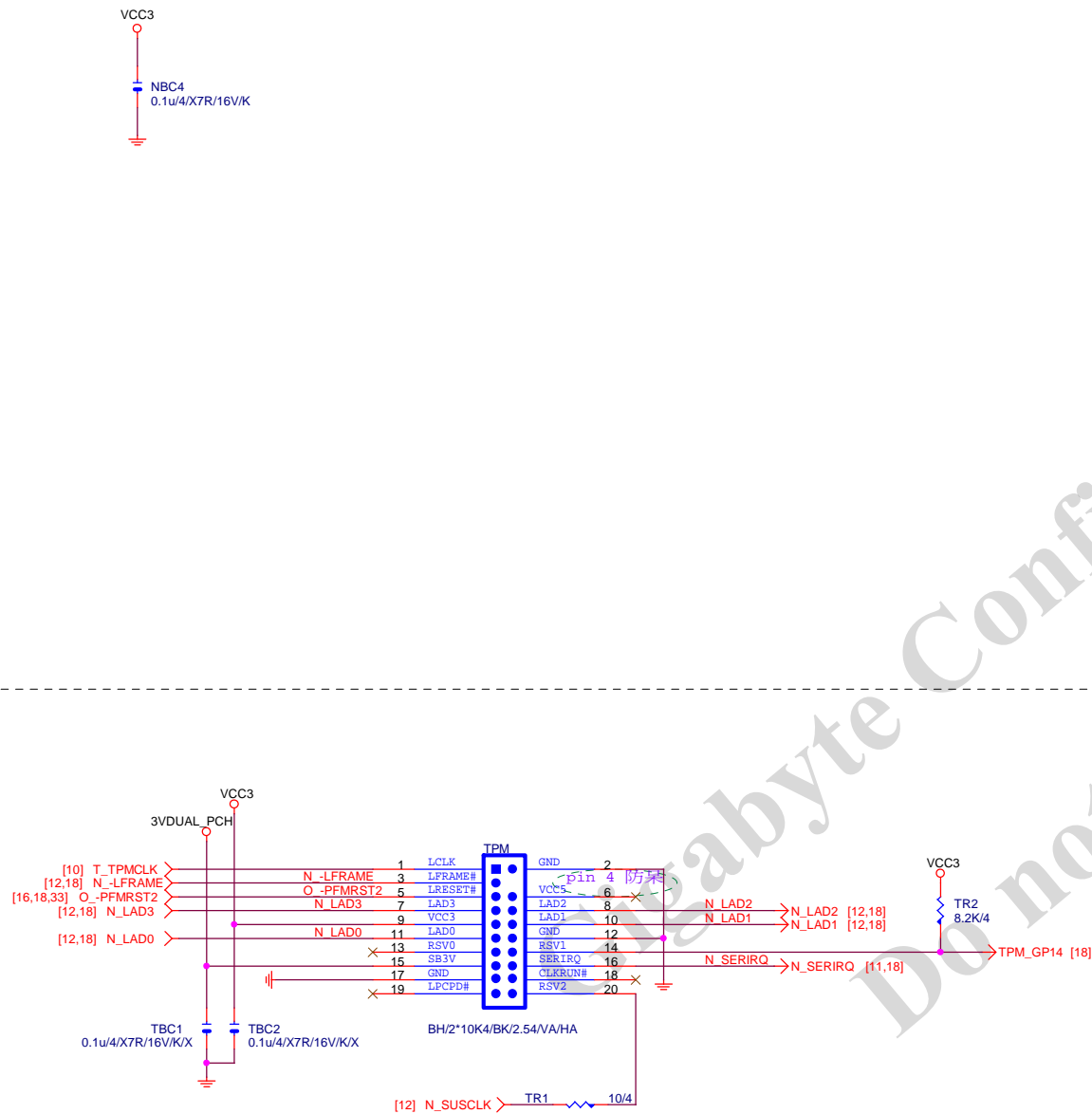
[4] A_-PROHOT ↔ A_-PROHOT

-PROHOT



Gigabyte Technology

Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number	Rev	
Custpm		GA-H77-D3H-MVP	
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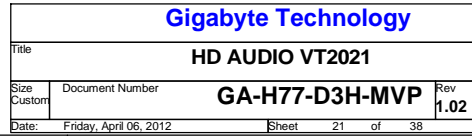
**Gigabyte Technology**

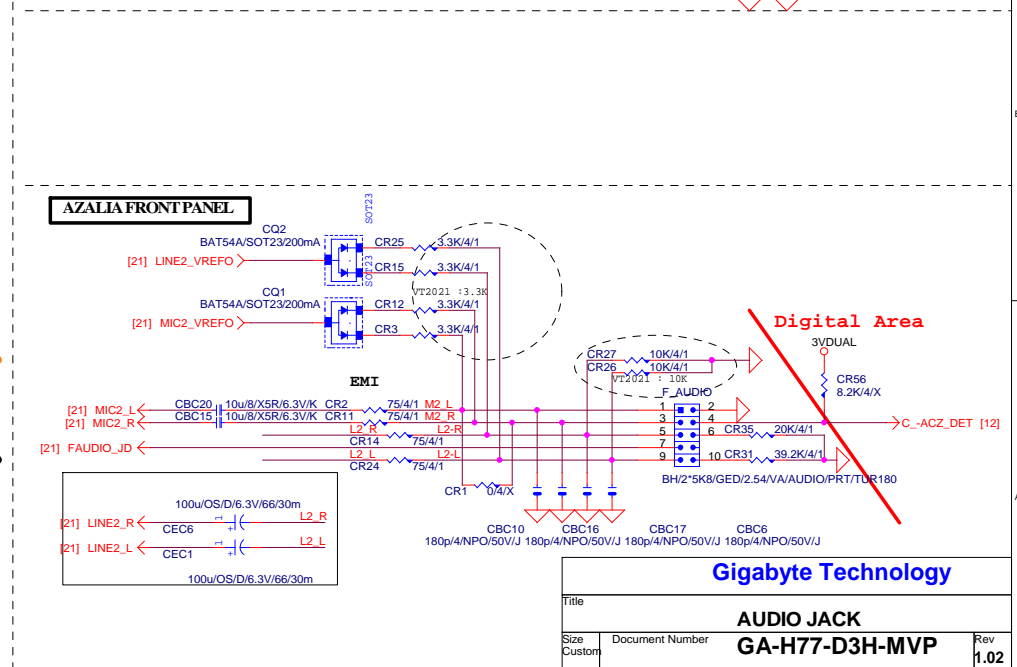
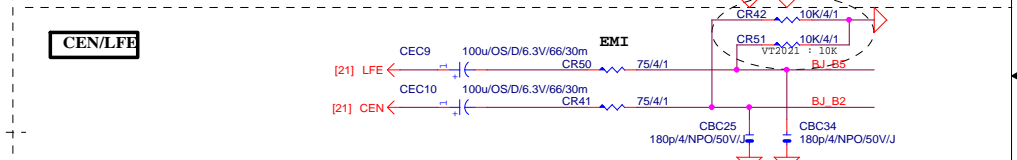
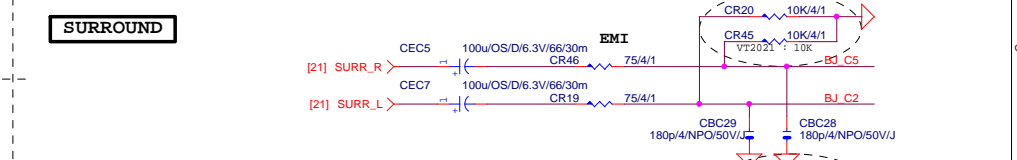
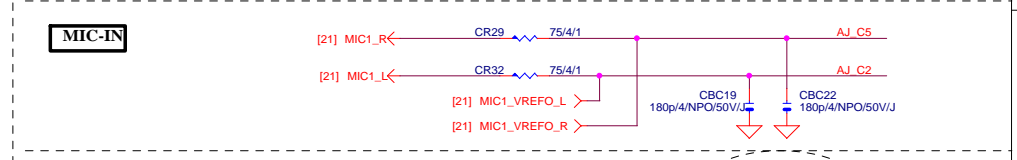
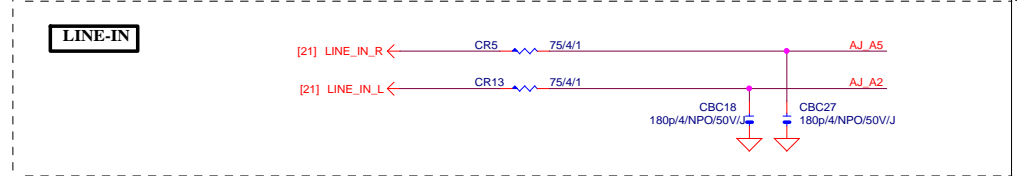
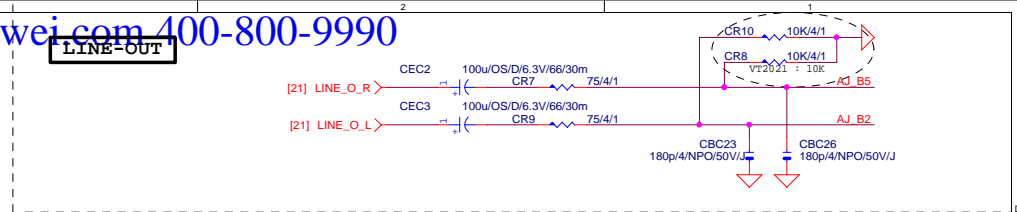
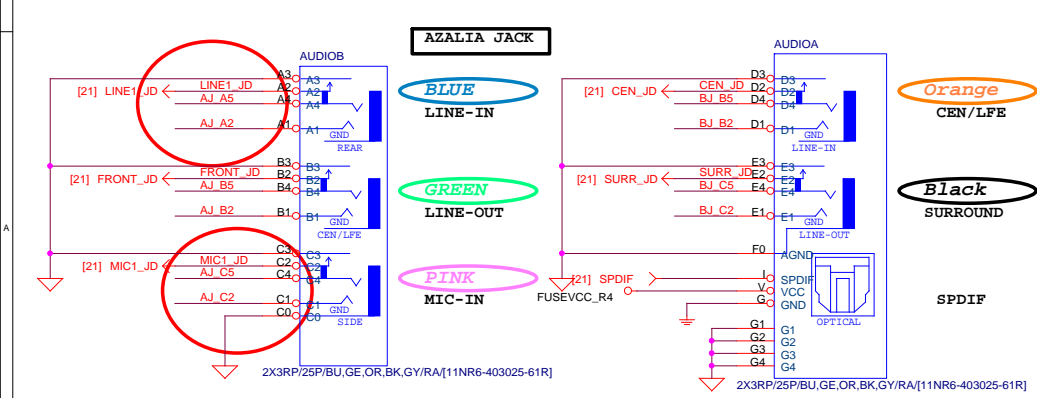
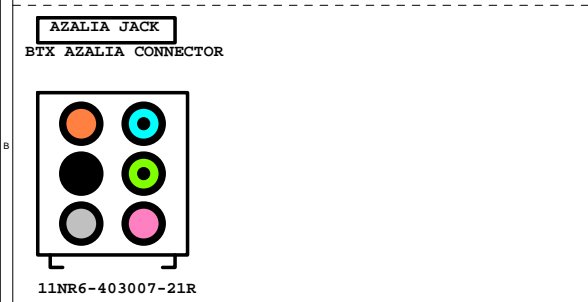
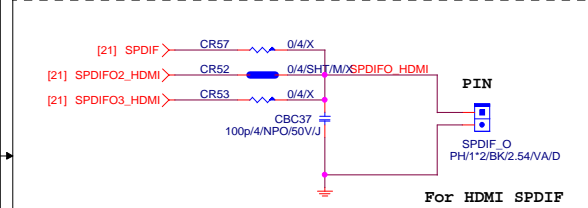
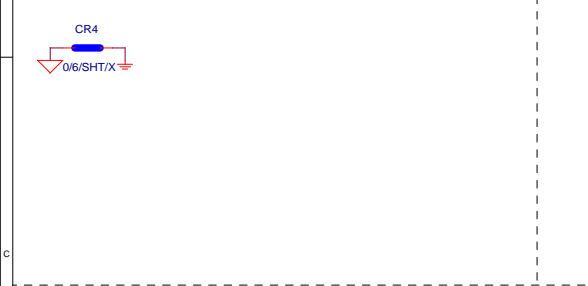
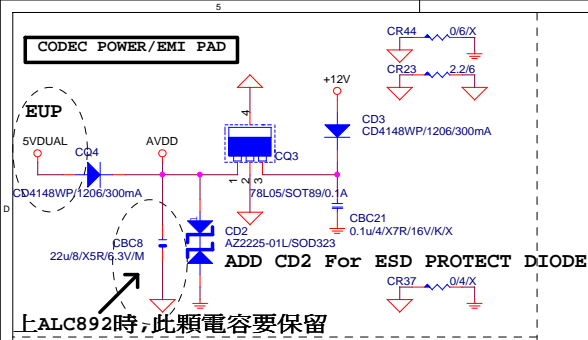
Title		BIOS	
Size	Document Number	GA-H77-D3H-MVP	Rev 1.02
Custom			
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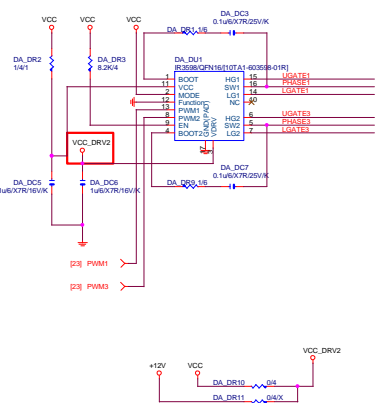
CR36: 20K/4/1 @Realtek cdec & VT1708S-CE
CR36: 51K/4/1 @VIA codec VT1708S-CD/VT2021
CBC38 100p @VIA codec VT1708S

CBC38 100p/4/NPO/50V/JXX

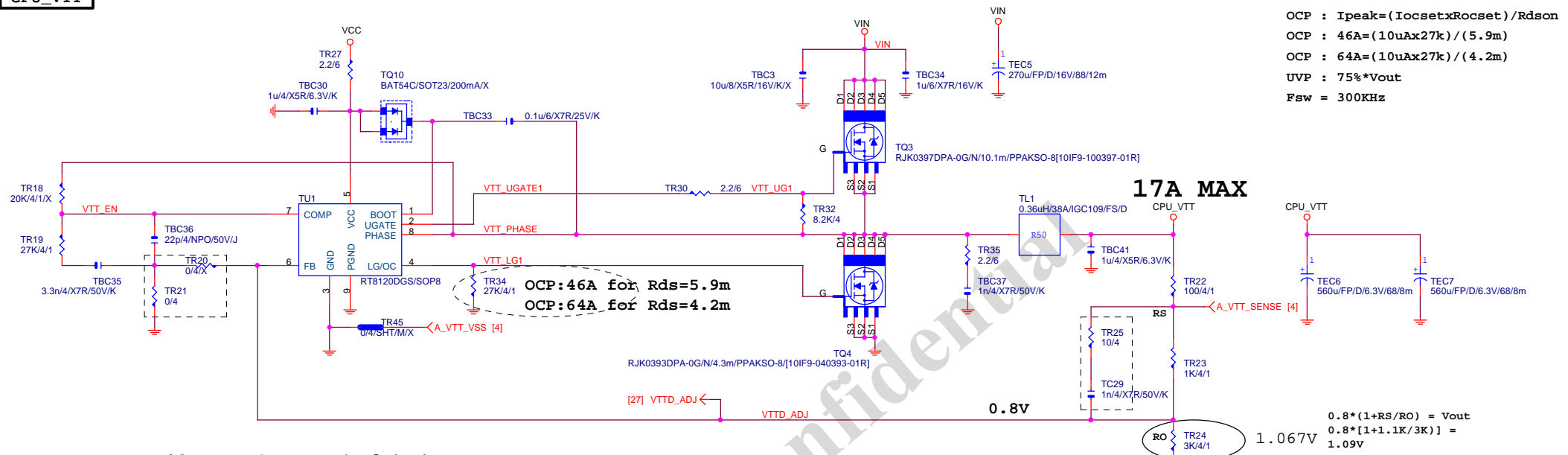
CR36 5.1K/4/1





VCORE Phase
1,3

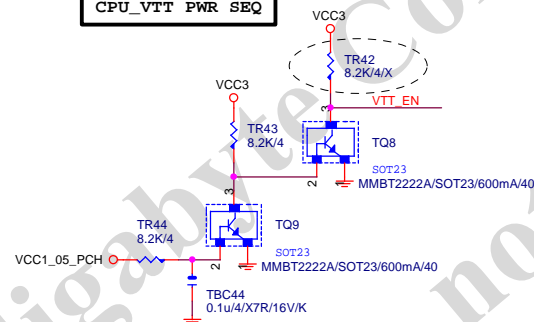
CPU_VTT



$$OCP: 46A = \frac{R_{oset} * I_{ocset}}{R_{ds}(on)}$$

$$= \frac{27K * 10uA}{5.9m}$$

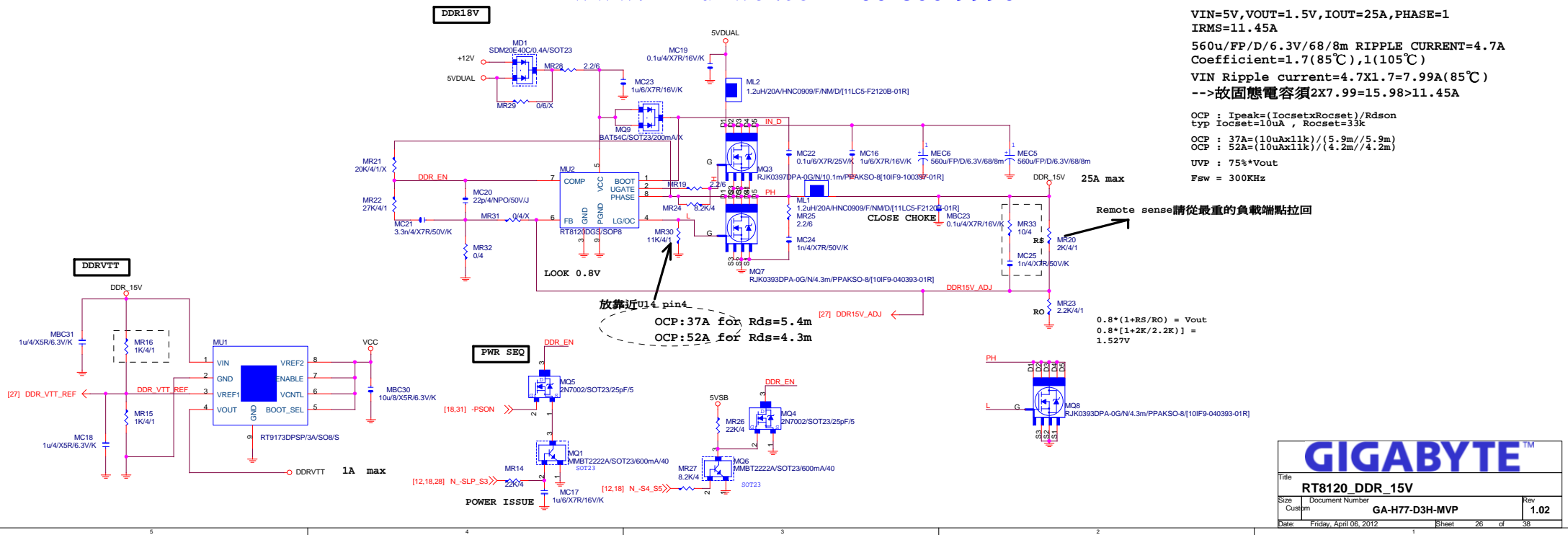
CPU_VTT PWR SEQ

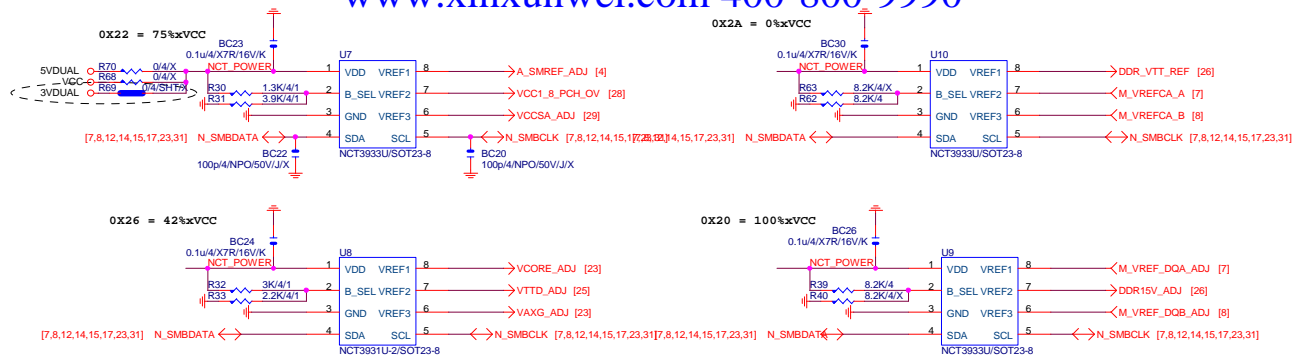


	VTT_SEL
HI	1.05V
LO	1.0V

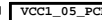
GIGABYTE™

Title RT8120 CPU_VTT			
Size Custom	Document Number GA-H77-D3H-MVP	Rev 1.02	
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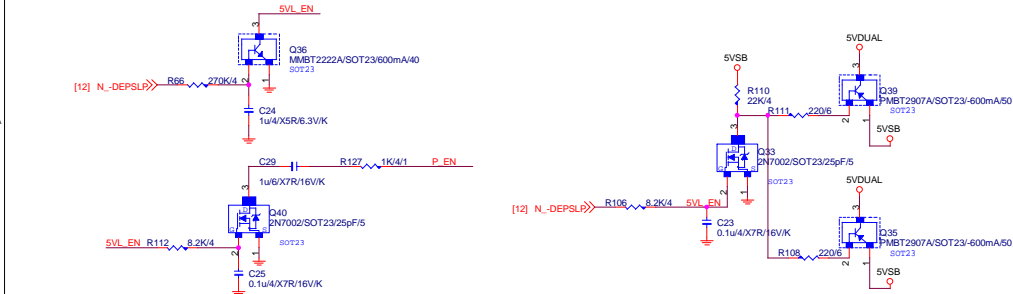
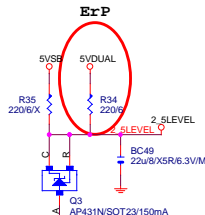
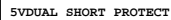


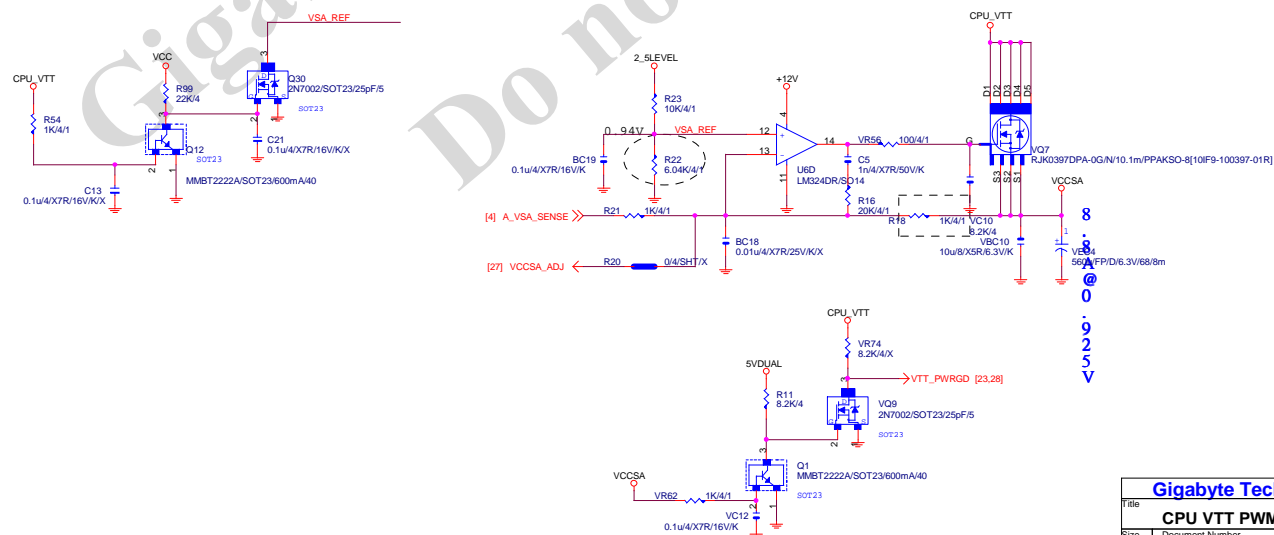
NCT3933	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	SMREF	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	CPU_VTT
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	VCCSA	VAXG

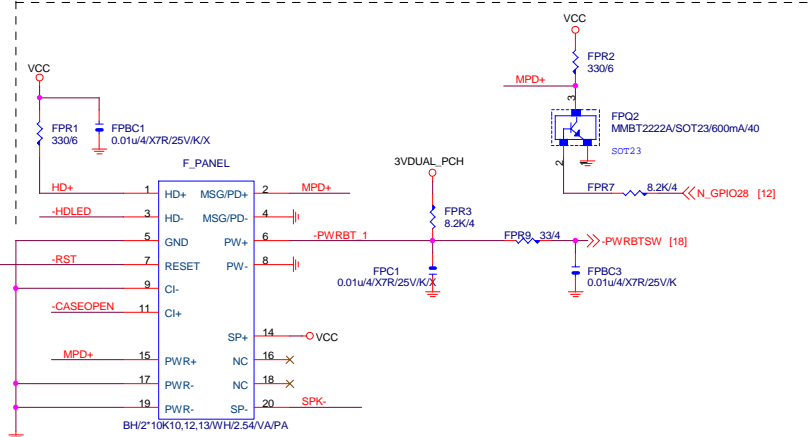
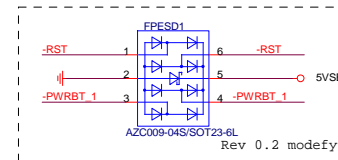
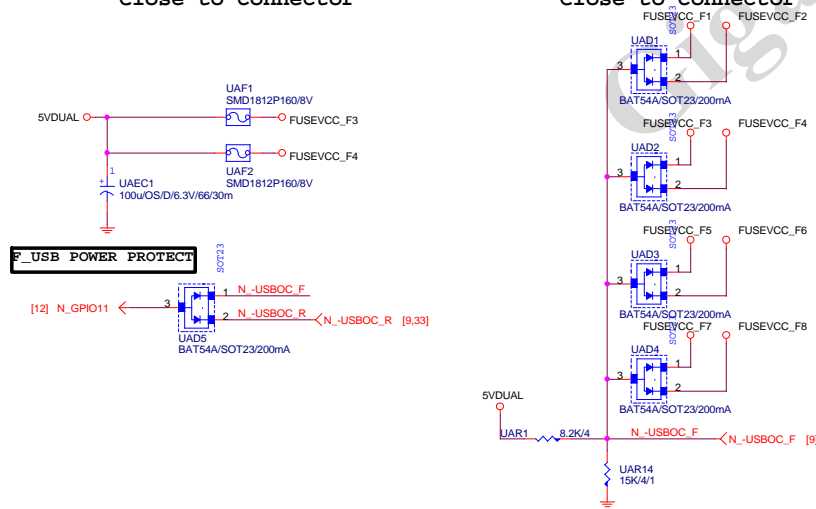
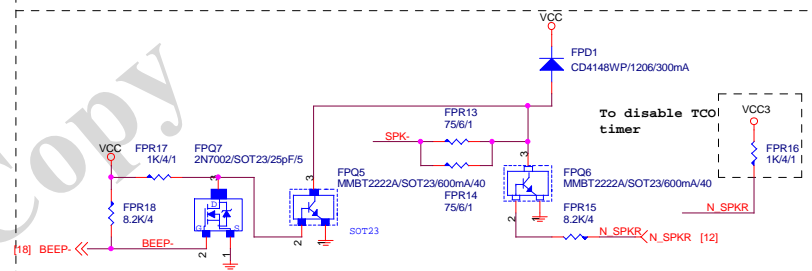
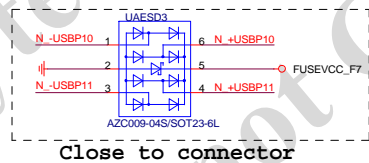
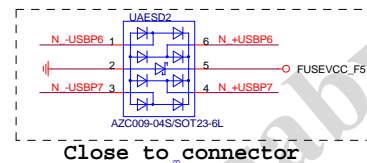
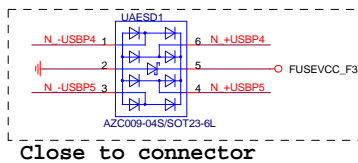
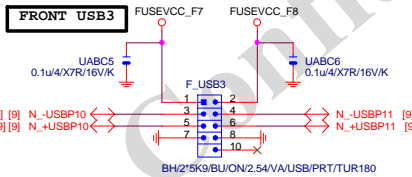
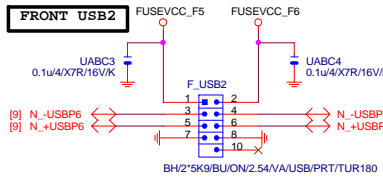
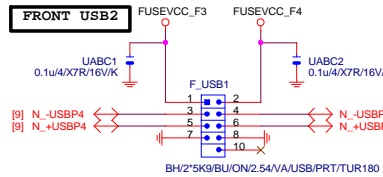
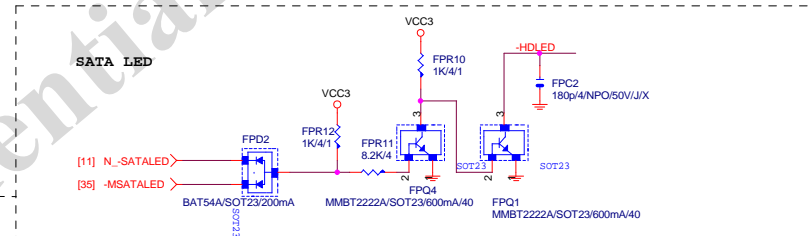
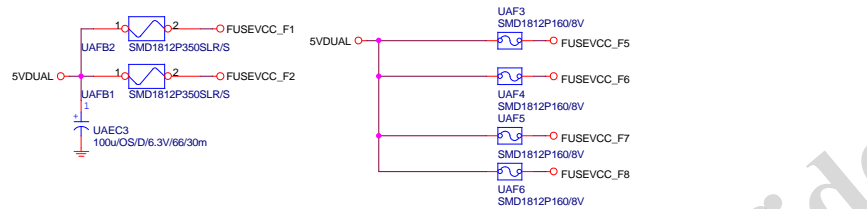
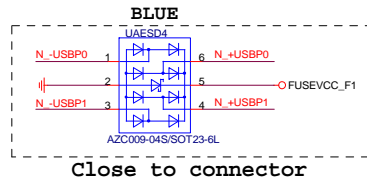
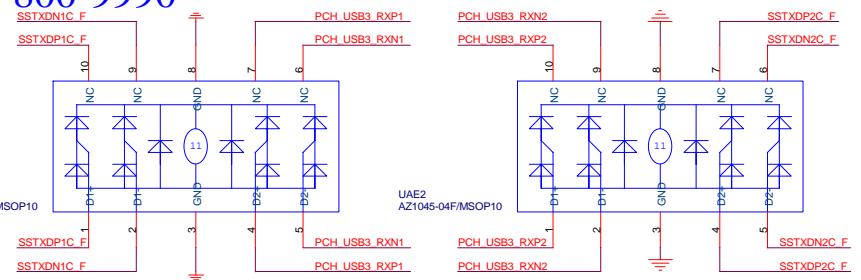
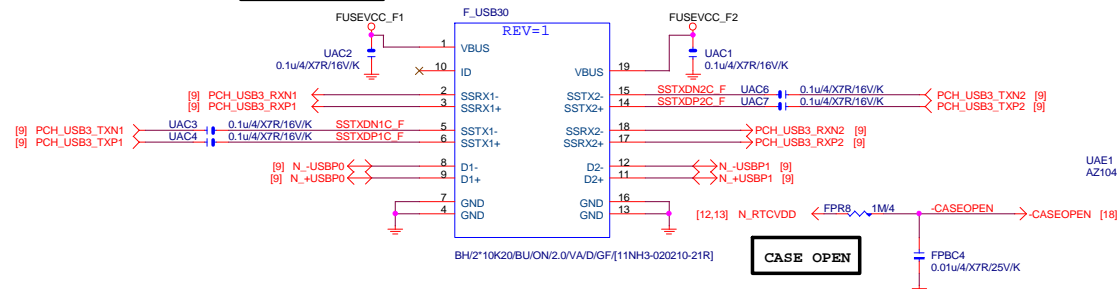


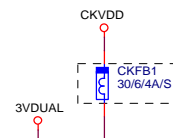
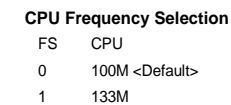
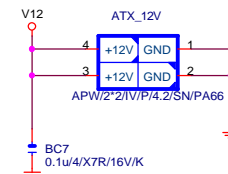
Title			
DISCRETE POWER			
Size C	Document Number	GA-H77-D3H-MVP	Rev 1.02
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PCH ErP Control

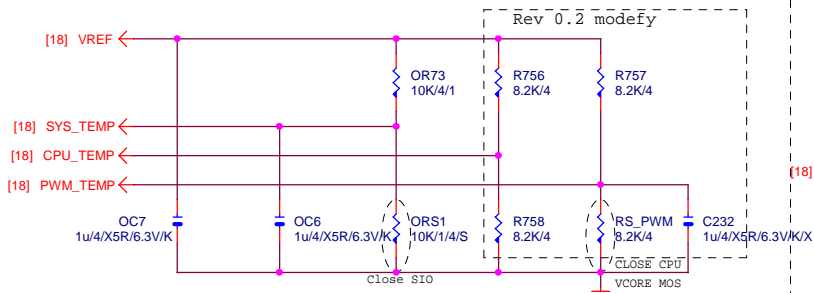




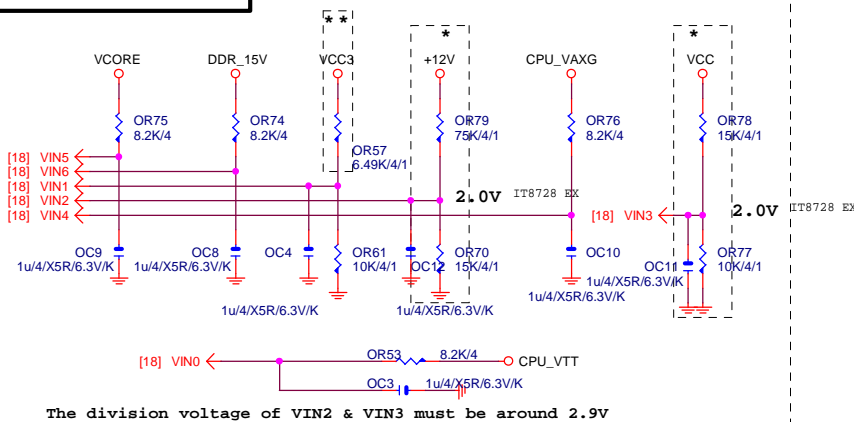




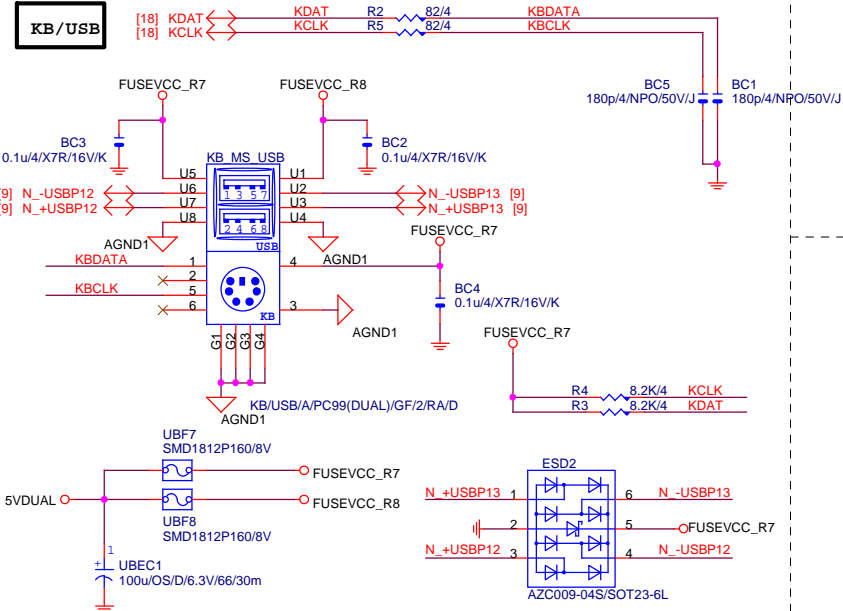
TEMP H/W MONITOR



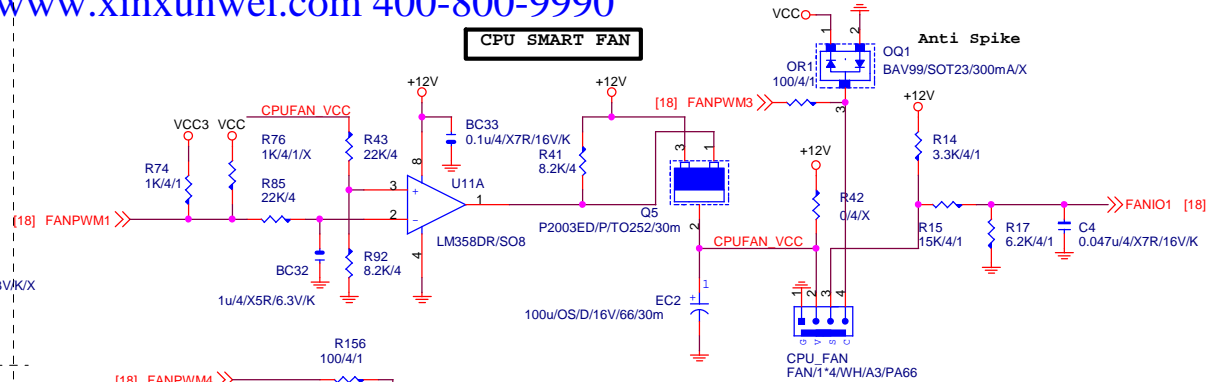
VOLTAGE-- H/W MONITOR



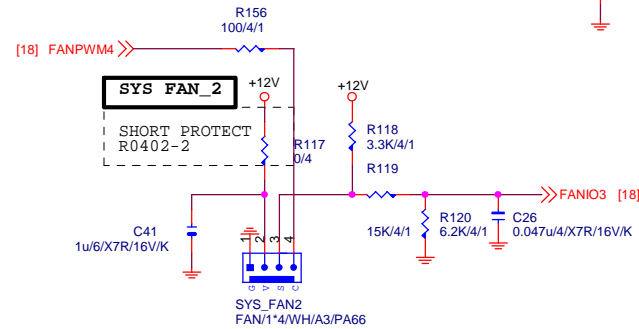
KB/USB



CPU SMART FAN

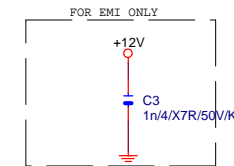
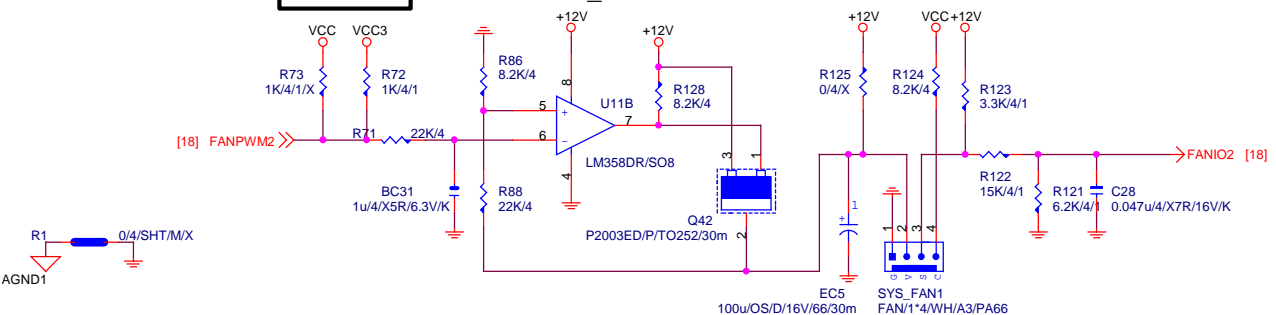


SYS FAN_2



SYS FAN_1

Linear SYS_FAN

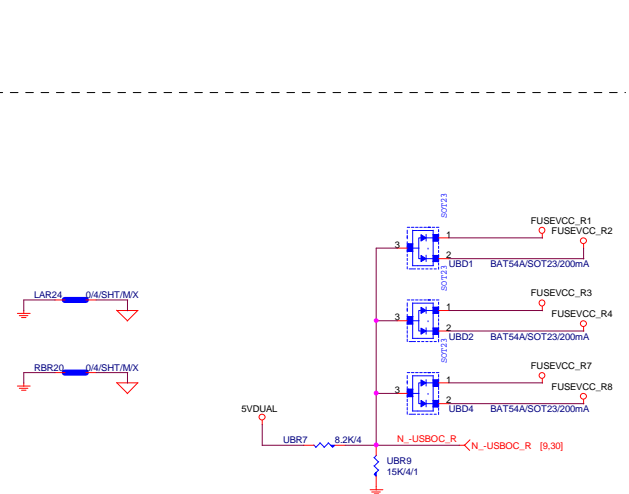
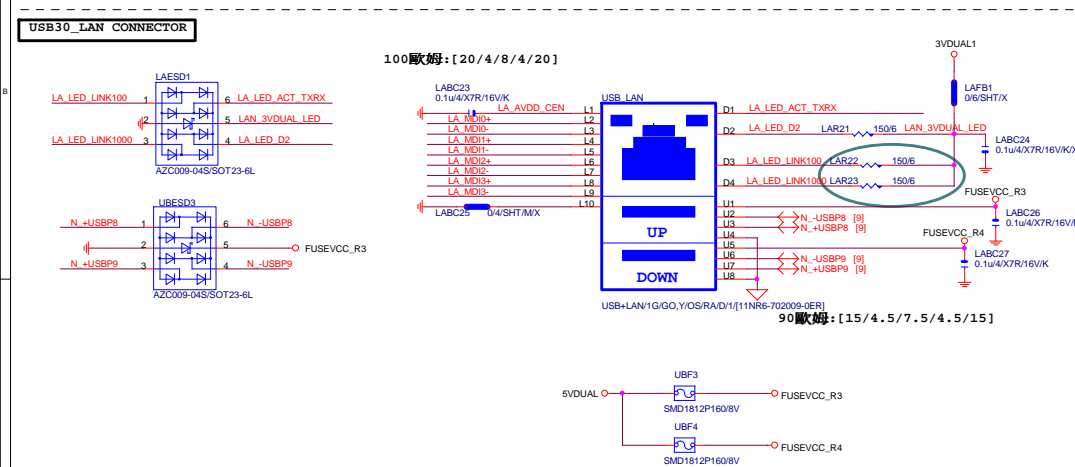
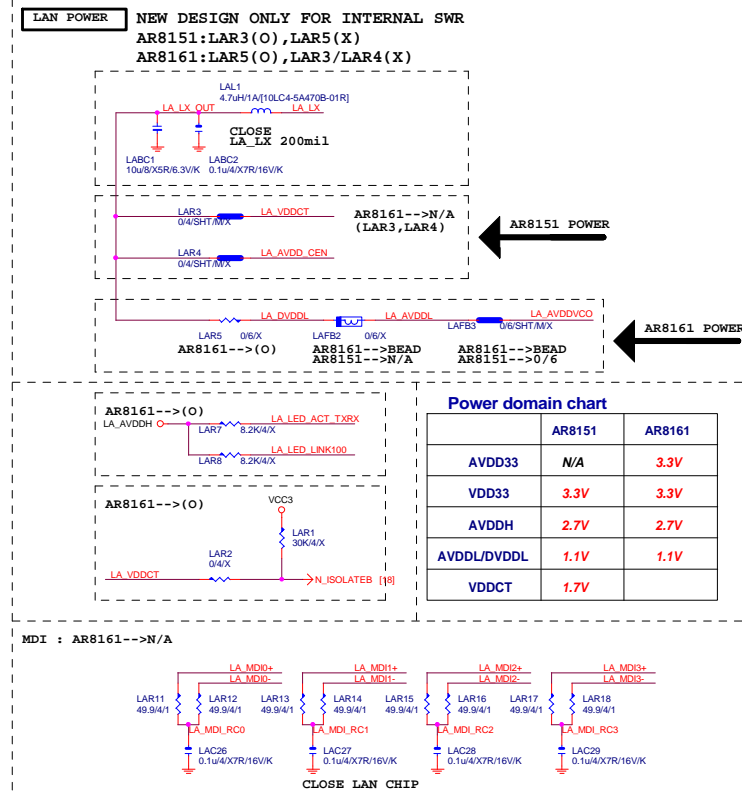
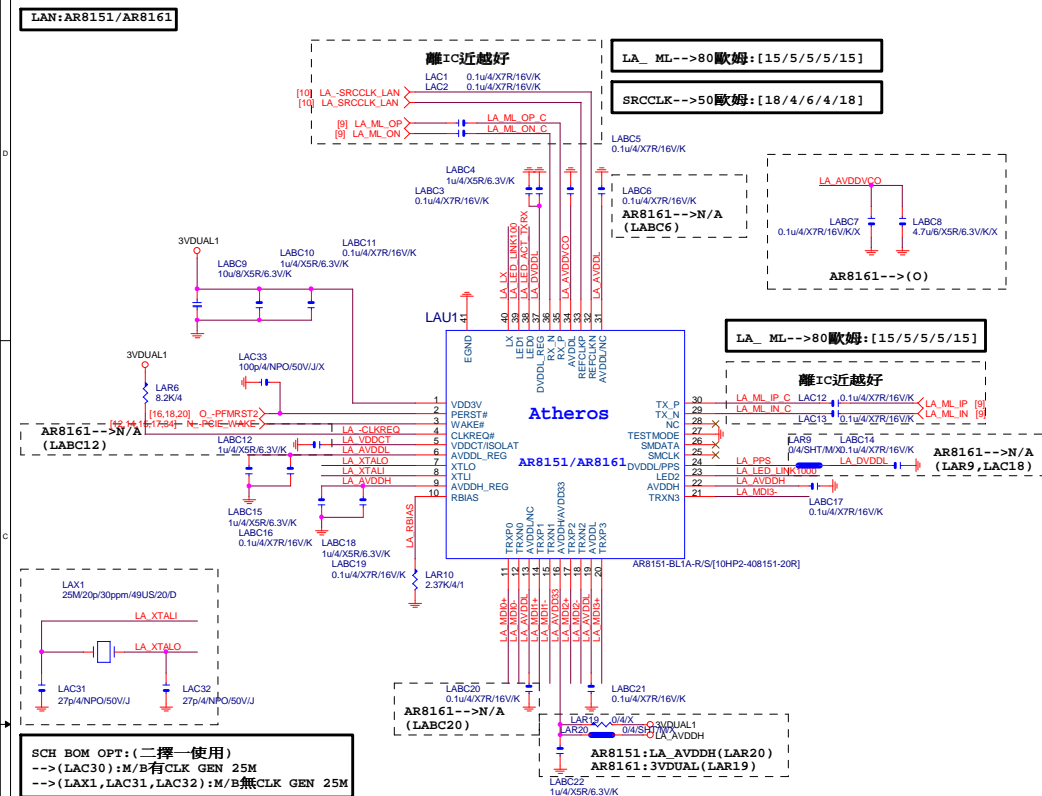


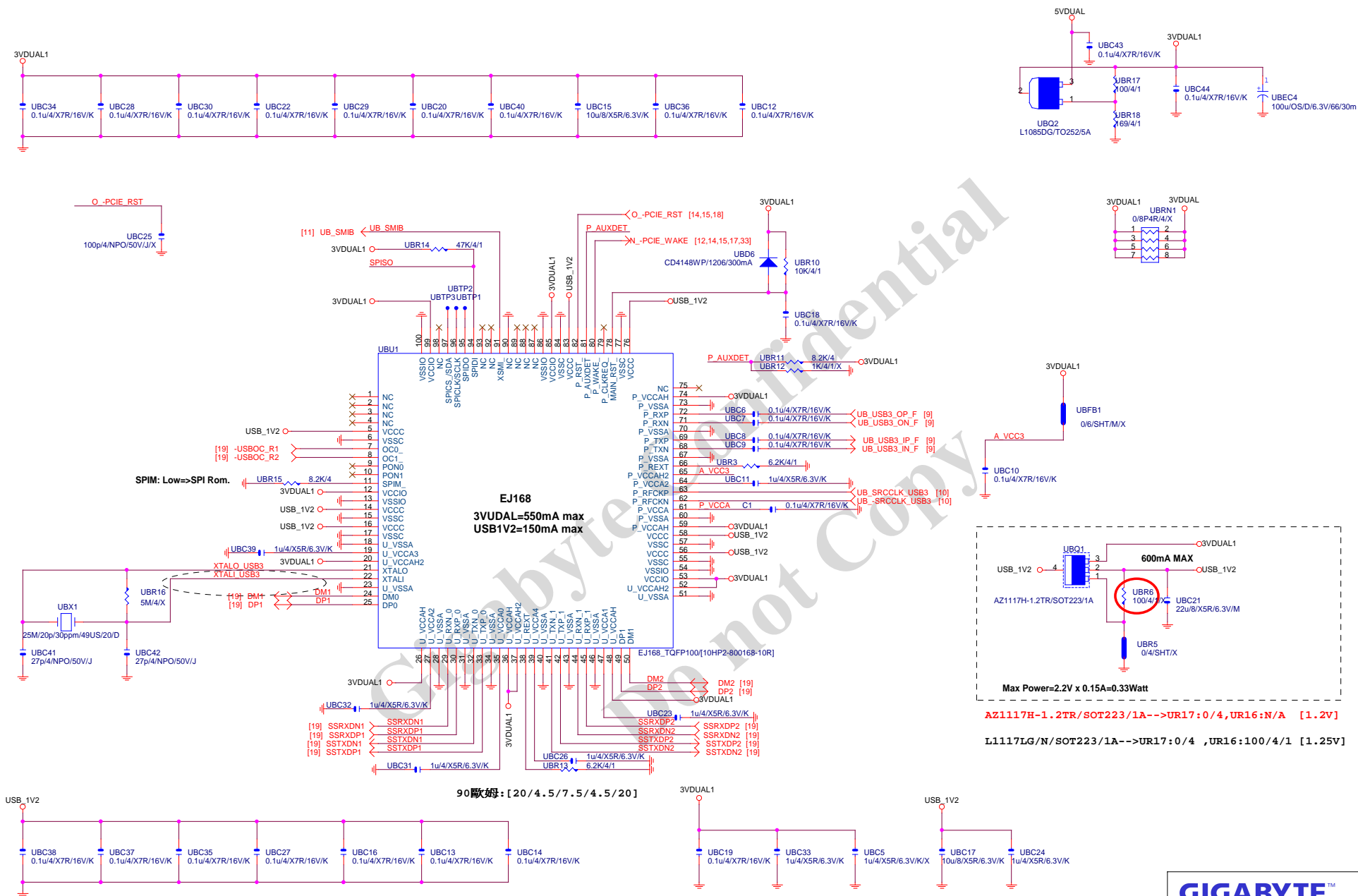
Gigabyte Technology

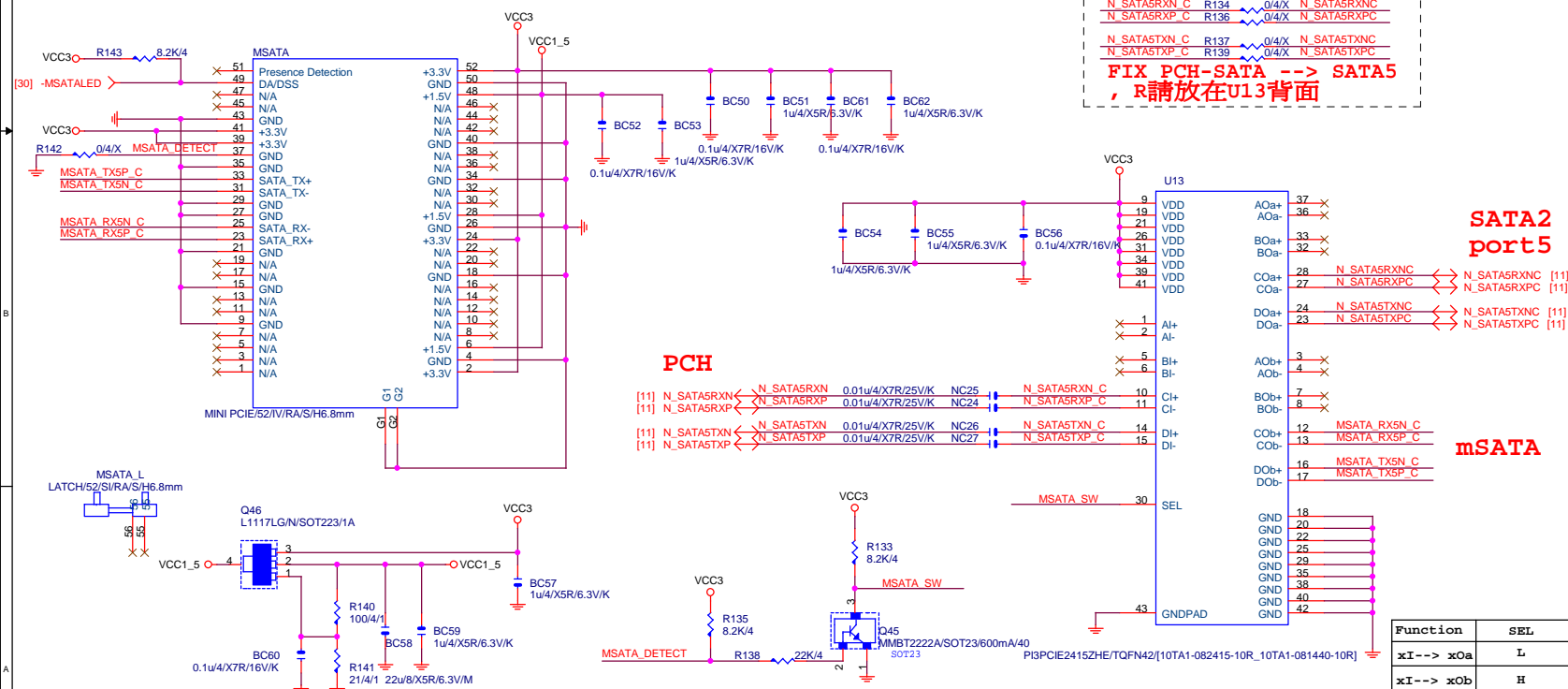
HWM,KB/MS, FAN CTRL

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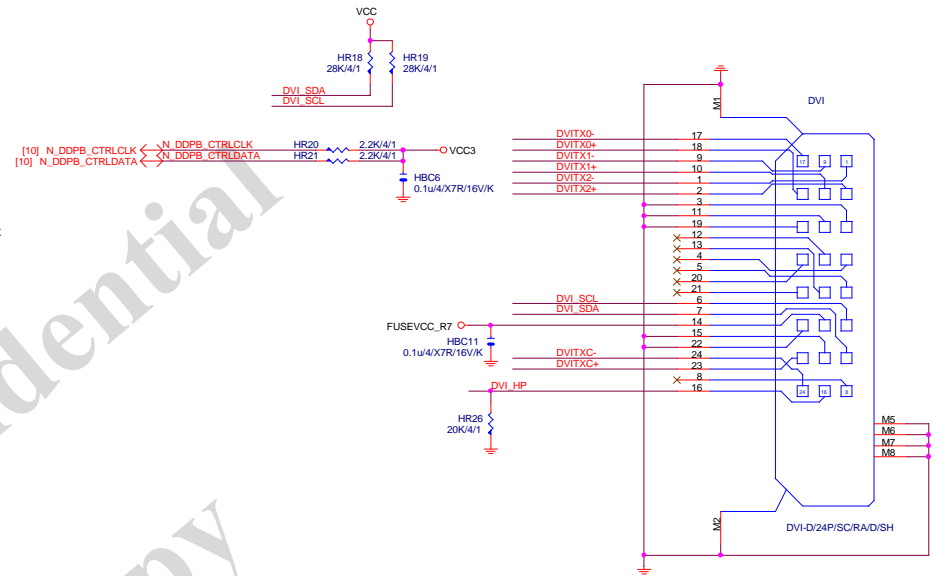


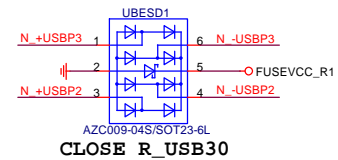
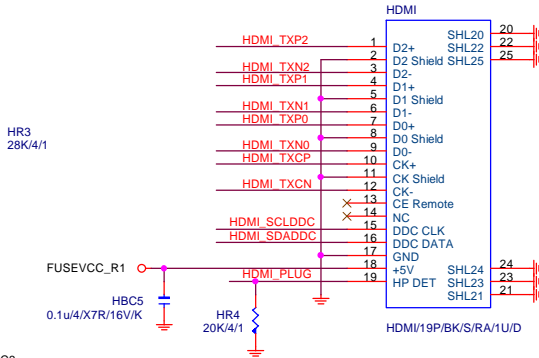
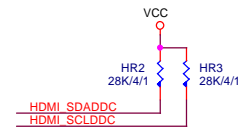
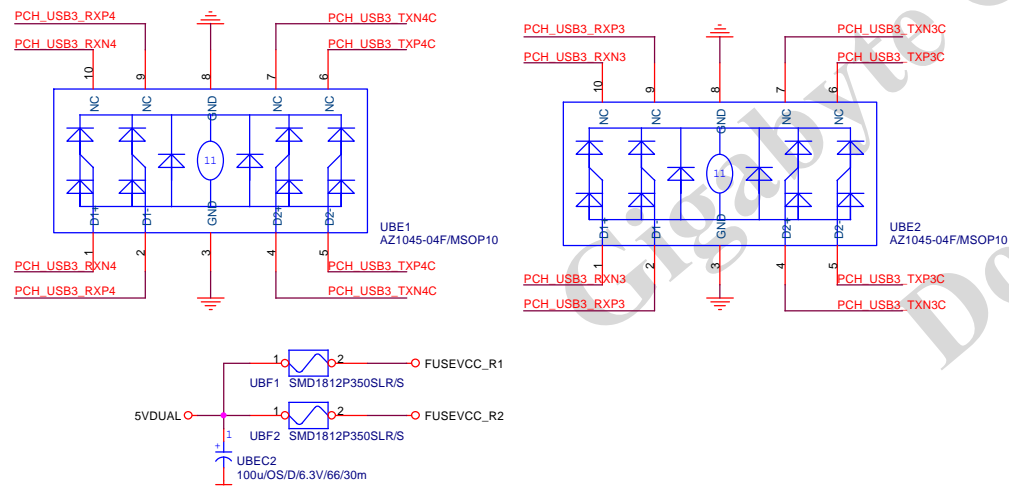
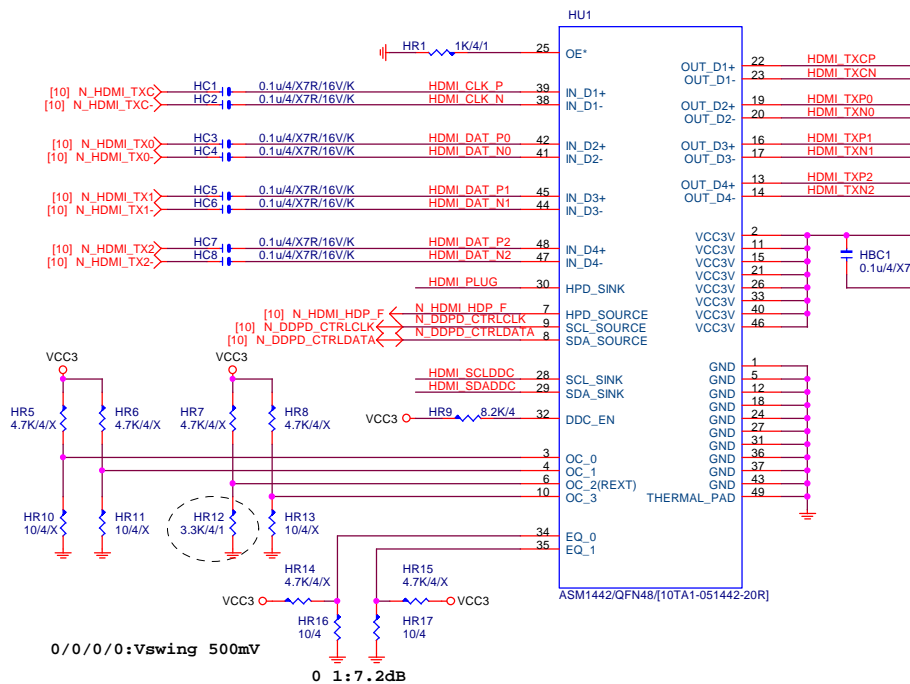




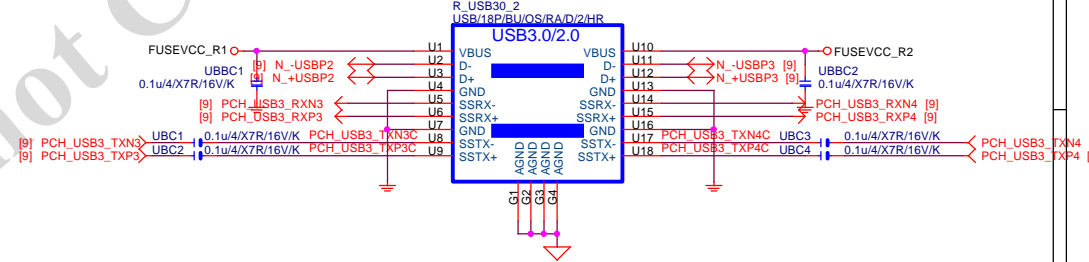
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USB30_20



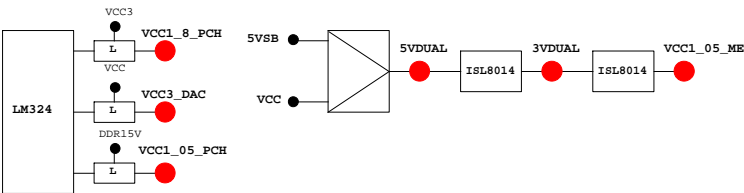
GIGABYTE™			
Title			
HDMI & USB			
Size	Document Number	Rev	
Custom	GA-H77-D3H-MVP	1.02	
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PCH GPIO LIST TABLE				
PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	-PECI_REQ	N/A
GP1/TACH1	MAIN		ICH_FAN_TACH1	N/A
GP2/PIRQ#	MAIN		-PIRQE	P/U 8.2K VCC3
GP3/PIRQ#	MAIN		-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#
GP10/OC6#	STBY		NATIVE	OC6#
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL
GP13	STBY	L	GPI	GPIO13
GP14/OC7#	STBY		NATIVE	OC7#
GP15	STBY	L	GPO	GPIO15
GP16	MAIN		GPI	-SKT0CC
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0
GP18	MAIN		NATIVE	MB_ID0
GP19	MAIN		GPI	-LAN1_ISO
GP20	MAIN		NATIVE	LED_CTL
GP21	MAIN		GPI	VCC18_FCH_OV2
GP22	MAIN	H-Z	GPI	VCORE_OV3
GP23	MAIN		NATIVE	-LDRQ1
GP24	STBY	L	GPO	TLS
GP25	STBY		NATIVE	-CPU_STOP
GP26	STBY		NATIVE	-ACZ_DET
GP27	STBY	H	GPO	GPIO27
GP28	STBY	H	GPO	GPIO28
GP29	STBY	L	GPI	GPIO29
GP30	STBY	H-Z	GPI	S_PWR_ACK
GP31	STBY	H-Z	GPI	N/A(Reverse)
GP32	MAIN	H	GPO	MB_ID1
GP33	MAIN	H	GPO	LOAD-LINE
GP34	MAIN	H-Z	GPI	-PCI_STOP
GP35	MAIN	L	GPO	GPIO35
GP36	MAIN		GPI	-LAN1_DSM
GP37	MAIN		GPI	N/A
GP38	MAIN	H-Z	GPI	VCORE_OV2
GP39	MAIN	H-Z	GPI	-LAN_DSM
GP40	STBY		NATIVE	OC1#
GP41	STBY		NATIVE	OC2#
GP42	STBY		NATIVE	OC3#
GP43	STBY		NATIVE	OC4#
GP44	STBY	L	NATIVE	N/A
GP45	STBY		NATIVE	-LPCPME
GP46	STBY	L	NATIVE	PWR_LED
GP47	STBY		NATIVE	PSI_LED
GP48	MAIN	H-Z	IN	EN_PWM
GP49	MAIN	H-Z	IN	VCC18_OV1
GP50	MAIN		NATIVE	-REQ1
GP51	MAIN	H	NATIVE	-GNT1
GP52	MAIN		NATIVE	-REQ2
GP53	MAIN	H	NATIVE	-GNT2
GP54	MAIN		NATIVE	-REQ3
GP55	MAIN	H	NATIVE	-GNT3
GP56	STBY		NATIVE	N/A(Reverse)
GP57	STBY	H-Z	IN	VCORE_OV1
GP58	STBY	H-Z	NATIVE	F_USB_OC
GP59	STBY		NATIVE	USB_OC0#
GP60	STBY	H-Z	NATIVE	N/A(Reverse)
GP61	STBY	L	NATIVE	-SUSTAT
GP62	STBY	L	NATIVE	SUSCLK
GP63	STBY	L	NATIVE	GPIO63
GP64	MAIN	L	NATIVE	CLKOUTFLEX0
GP65	MAIN	L	NATIVE	CLKOUTFLEX1
GP66	MAIN	L	NATIVE	CLKOUTFLEX2
GP67	MAIN	L	NATIVE	CLKOUTFLEX3
GP72	STBY	H-Z	NATIVE	VCORE_OV4
GP73	STBY		NATIVE	1_05V_OV1
GP74	STBY	H-Z	NATIVE	1_05V_OV2
GP75	STBY	H-Z	NATIVE	N/A(Reverse)

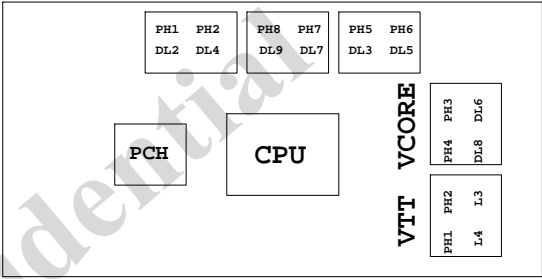
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
Title	TABLE LIST		
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